# Characterization of Metrological Grade Analog-to-Digital Converters Using a Programmable Josephson Voltage Standard

Frédéric Overney, *Member, IEEE*, Alain Rüfenacht, Jean-Pierre Braun, *Member, IEEE*, Blaise Jeanneret, and Paul S. Wright

***Abstract*—A test bench has been developed for systematic characterization of high-resolution analog-to-digital converters. The reference signal is generated by a programable Josephson voltage standard. Three 24-bit digitizers have been characterized. Noise performance has been measured at direct current using the Allan deviation, whereas integral nonlinearity has been measured with quasi-dynamic stepwise triangular waveforms at frequencies between 0.5 Hz and 1 kHz. None of the digitizers outperforms all others for each tested characteristics. Therefore, such a systematic characterization provides the overview needed to identify the most suitable digitizer for a given application.**

***Index Terms*—Analog-digital conversion, delta–sigma modulation, Josephson junctions, metrology, noise measurement.**

## I. Introduction

THE STEADY improvement of analog-to-digital converter (ADC) technology has led to the apparition of commercial devices with 24-bit of resolution and sampling rates up to 500 kS/s. Such ADCs are particularly well suited for metrological applications such as impedance calibration by a sampling technique [1], development of Josephson-locked sine-wave synthesizer [2], [3], and electrical power measurements [4], [5]. These applications require high resolution and a bandwidth up to 10 kHz. However, to ensure traceable measurements, these converters must be characterized with adequate accuracy.

Test methods for ADCs were developed many years ago and were fully standardized (IEEE Std. 1241-2000 and IEEE Std. 1057-2007 [6], [7]). However, one of the limitation of these test methods for high-resolution ADCs resides in the relatively low accuracy of reference voltages applied to high-resolution digitizers. The use of a programmable Josephson voltage standard (PJVS) [8] permits to overcome this limitation and enables the development of new methods for characterization of digitizers with the highest level of accuracy [9], [10]. In addition, the PJVS intrinsically ensures the traceability of the measurements.

To this end, a test bench for the direct- and alternating-current (ac and dc, respectively) characterizations of metrological grade ADCs has been developed [11] around a PJVS of 1 V. The principle is to apply the known voltage of the PJVS output to an ADC's input. Due to the intrinsic accuracy of the Josephson voltage, any difference between the applied voltage and the ADC reading is solely related to an ADC error.

The PJVS has already been successfully used for the characterization of digitizers [9], [10], [12]. However, the present test bench is particularly well suited for the systematic characterization of ADCs under various conditions.

In this paper, the results of the characterization of three different metrological grade ADCs are presented. Two types of characterization have been carried out with a Josephson reference voltage: dc characterization, where a dc Josephson signal is applied to the input of an ADC, and quasi-dynamic characterization, where a stepwise triangular Josephson signal is applied to the input of the ADC. The term quasi-dynamic refers, in this paper, to the fact that signals are made up by successive steps as opposed to continuously varying.

## II. Description of the Test Bench

The schematic of the Josephson-based test bench is shown in Fig. 1. The PJVS supplies the reference voltage waveforms directly to the digitizer under test (DUT). The design and operation of the PJVS, which is based on a superconductor–insulator–normal-metal–insulator–superconductor Josephson junction array, is fully described in [13]. In this paper, the maximum voltage provided by the 8192 Josephson junction array at 70 GHz is only 1.18 V. Therefore, only a fraction of the digitizer's full-scale range (FSR) can be tested when the FS is bigger than 1 V (see Table I). To overcome this limitation, a new current source is under development and will be able to drive a 10-V Josephson junction array [14].

Both the PJVS and the DUT are frequency locked to the same reference signal of 10 MHz provided by a Cs clock. Moreover, the programmable Josephson bias current source supplies the trigger signal to synchronize the digitizer to the Josephson stepwise waveform. Both the clock and the trigger signals are optically distributed to avoid spurious coupling between the various components of the system.

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F. Overney, A. Rüfenacht, J.-P. Braun, and B. Jeanneret are with the Federal Office of Metrology (METAS), Bern-Wabern 3003, Switzerland (e-mail: frederic.overney@metas.ch).

P. S. Wright is with the National Physical Laboratory, Teddington TW11 0LW, U.K.

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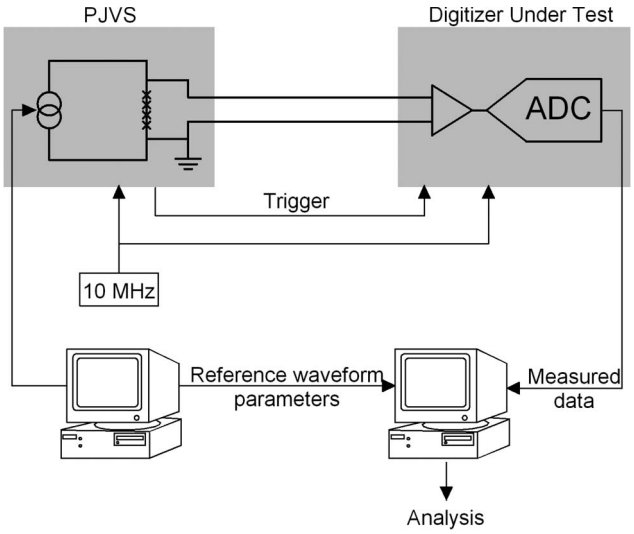


Fig. 1. Schematic of the test bench using the PJVS to generate the reference signal measured by the DUT.

TABLE I
LIST OF THE MAIN SPECIFICATION OF THE THREE DIGITIZERS EVALUATED IN THIS PAPER

| Name | Sampling rate kS/s | Resolution bit | FS V | Ref. |
|---|---|---|---|---|
| NI5922 | 500<br>1000<br>5000 | 24<br>22<br>20 | 1 or 5 | [15] |
| NI4461 | 204.8 | 24 | 1, 3.16 or 10 | [16] |
| NPL7767 | 32 | 24 | 1.5 | [17], [18] |

The first computer is dedicated to fully control the reference voltage generated by the PJVS. Reference waveform parameters are sent to the second computer, which also gathers the measured data from the digitizer for further analysis.

## III. DEVICES UNDER TEST

Three different digitizers have been characterized: two commercial products based on a delta–sigma ADC and one system designed by the National Physics Laboratory (NPL) around an oversampled successive approximation ADC.

Conceptually, a digitizer contains different key components such as an input amplifier, analog and digital filters, and the ADC itself. Since only limited information about the precise architecture inside each digitizer is available, they are considered as black boxes. Therefore, the error of the digitizer is the difference between an input signal and an ADC's output. Throughout this paper, the terms digitizer or ADC are used interchangeably.

Table I summarizes the main characteristics of the digitizers evaluated in this paper. For a more detailed description, the reader should refer to [15]–[18].

Two of the characterized digitizers are National Instrument (NI) PXI-boards mounted in a NI PXI-1036DC chassis, which also contains a timing module (NI PXI-6652) for synchronization. An external 10 MHz time base is connected to the PXI chassis through an optical link.

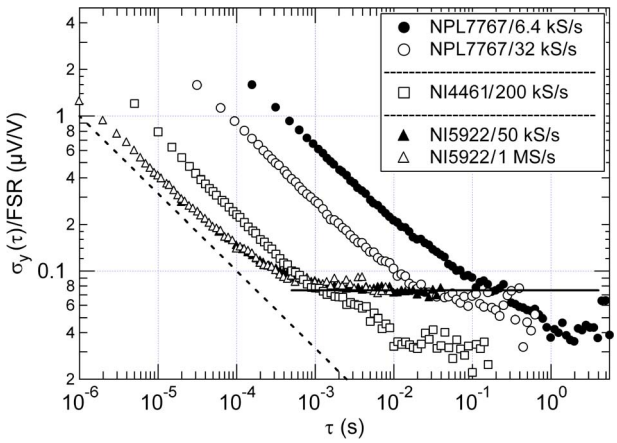


Fig. 2. Normalized Allan deviation representing intrinsic noise of the different digitizers. The dashed line is the characteristic of white noise (slope of $-1/2$), and the solid line represents the $1/f$ noise floor. These lines are guides for eyes.

The NI PXI-5922 board (named hereafter as NI5922) is a flexible resolution digitizer that can be used to acquire data with sampling rates from 50 kS/s to 15 MS/s.

The NI PXI-4461 board (named hereafter as NI4461) is a dynamic signal acquisition device having a resolution of 24-bit with sampling rates up to 204.8 kS/s.

The third digitizer (named hereafter as NPL7767) is a system designed by NPL around a commercial 24-bit successive approximation ADC having, in this case, a maximum sampling frequency of 32 kS/s. The NPL implementation includes signal-conditioning amplifiers to allow a $\pm 1.5$ FS single-ended input as well as an active antialiasing filter.

As listed in Table I, the digitizers have different FSRs. In every case, the FSR is symmetric around zero and spans the range from $-$FS to $+$FS. Therefore, FSR $= 2 \cdot$ FS.

## IV. NOISE CHARACTERIZATION

Fig. 2 shows the normalized (i.e., divided by the FSR) Allan deviation computed on a data sets acquired with a 50-$\Omega$ termination at the input of the digitizer. This measurement gives the intrinsic noise of the digitizer. Each digitizer shows the same behavior characterized by white noise (slope of $-1/2$) for a short measuring time followed by a $1/f$ noise floor for a longer measuring time.

Fig. 3 shows the white noise level extracted from Fig. 2 as a function of the sampling frequency. The white noise of the two NI digitizers is independent of the sampling frequency. Therefore, for a given measuring time, the uncertainty on the mean value of a small data set acquired with a small sampling rate is equivalent to the uncertainty on the mean value of a larger data set acquired with a higher sampling rate. For the NPL7767 digitizer, the white noise level decreases when the sampling rate increases. Therefore, from the uncertainty point of view, it is better to measure at the highest sampling rate and then take the mean value of the larger data set. Even in the best situation (sampling rate of 32 kS/s), the white noise level of NPL7767 is almost one order of magnitude larger than the white noise of NI5922. For the two NI digitizers, normalized white noise is slightly smaller for larger FSR settings.

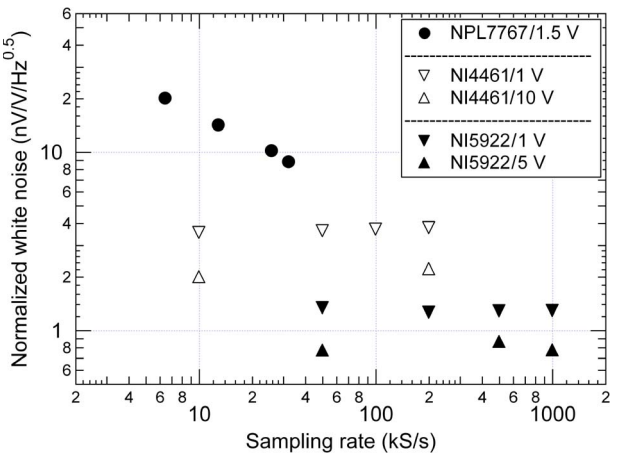


Fig. 3. Normalized white noise of the different ADCs as a function of the sampling frequency.

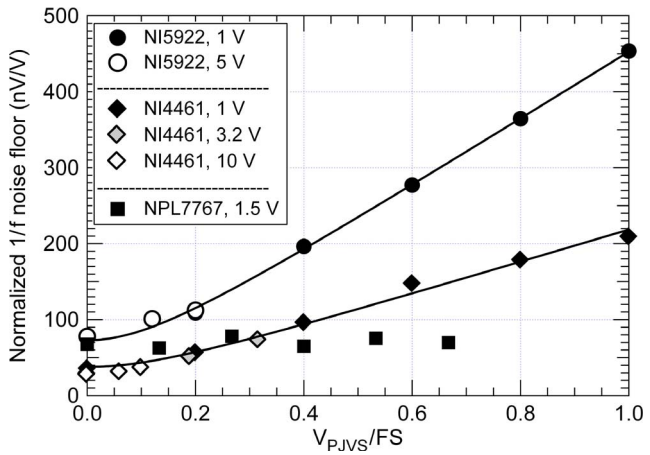


Fig. 4. Normalized $1/f$ noise floor versus normalized applied dc voltage. The lines are the least square fit of the value measured on the 1 V range of NI5922 and NI4461.

The Allan deviation measurements have been repeated with the application of a Josephson dc voltage at the digitizer's input instead of the 50 Ω termination. The voltage level has been set from 0 to 1 V. The voltage level applied to the digitizers has no effect on the white noise level. However, for the two NI boards, the $1/f$ noise floor clearly increases with the voltage level. The $1/f$ noise floor is reached after a measuring time from 50 to 100 ms for NI5922 and NI4461 and after 1 to 2 s for NPL7767. Therefore, no improvement of the type-A uncertainty can be expected by increasing the measuring time beyond these limits.

Fig. 4 shows the normalized $1/f$ noise floor as a function of the voltage level $V_{\mathrm{PJVS}}$ normalized to the FS. For the two NI digitizers, the $1/f$ noise level clearly increases with the voltage level. Such a behavior can be explained by assuming two sources of noise: One is related to offset $N_O$, and the other to gain $N_G$ of the digitizer. In this case, the total noise level is given by $\sqrt{N_O^2 + N_G^2 \cdot V_{\mathrm{PJVS}}^2}$. Due to the quantum nature of the Josephson effect, no noise is attributed to $V_{\mathrm{PJVS}}$. A small noise contribution could be attributed to thermal voltages along the connecting cables. This contribution should not be larger than the smallest noise level and can be neglected.

TABLE II
NORMALIZED NOISE CONTRIBUTION DUE TO THE OFFSET AND THE GAIN OF THE DIGITIZER

| Name | $N_O$/FSR nV/V | $N_G$/FSR nV/V/V |
|---|---|---|
| NI5922 | 73±4 | 447±3 |
| NI4461 | 38±7 | 215±6 |
| NPL7767 | 68±4 | 35±34 |

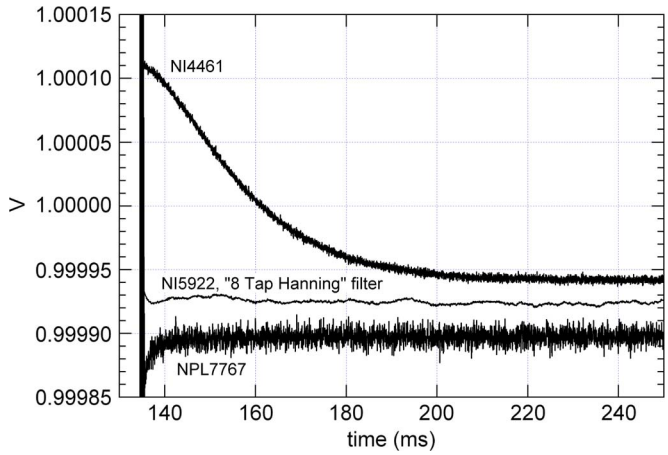


Fig. 5. Response of the digitizers to a quick change of the input voltage from 0 to 1 V. The nominal FS is 1 V for two NI ADCs and 1.5 V for the NPL digitizer.

Table II summarizes the noise levels $N_O$ and $N_G$ measured on the different digitizers. For a small input signal, noise is dominated by $N_O$, and the three digitizers show similar performances. For a larger input signal, noise is dominated by $N_G$ and therefore increases with the signal amplitude for the two NI boards. In comparison, the NPL digitizer presents a smaller noise source, which is mainly independent of the input signal amplitude.

## V. STEP RISING SHAPE

The response of the digitizer to a quick change of the input signal has also been investigated. For this purpose, successive pulses from zero to $V_{\mathrm{PJVS}}$ and back to zero have been generated by the PJVS. The amplitude, $V_{\mathrm{PJVS}}$, of the pulse has been varied from 0.1 to 1 V by an increment of 0.1 V. Fig. 5 shows the response of the different digitizers to a rapid change of the input voltage from 0 to 1 V. The sampling frequency was 50 kS/s for the two NI boards and 30 kS/s for the NPL digitizer.

The digitizer NI4461 shows a large overshoot following the quick change of the input voltage and needs a few tens of millisecond to recover a steady state. The amplitude of the overshoot depends on the pulse amplitude $V_{\mathrm{PJVS}}$ and becomes observable only for a pulse amplitude greater than 0.4 V on the 2-V FSR. Such an overshoot is not visible for the other digitizers.

For NPL7767, the digitizer requires a few millisecond to reach the steady state when the pulse amplitude is higher than 0.4 V. For smaller pulse amplitudes, a settling time less than a millisecond is observed.

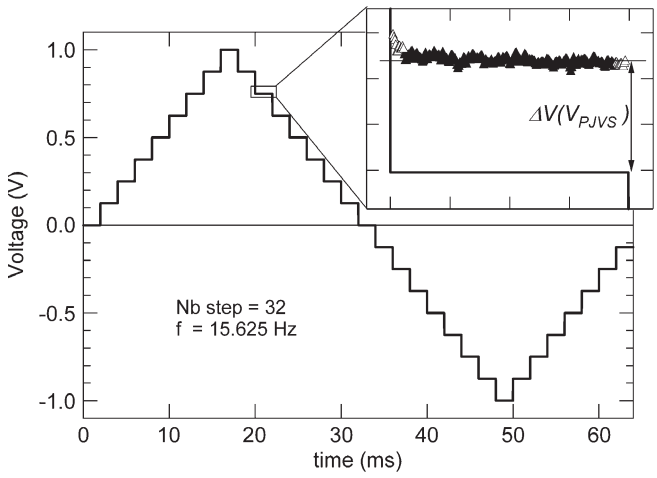


Fig. 6. Stepwise triangular reference waveform generated by the PJVS (solid line) and the corresponding digitized waveform (symbols). The inset shows that the values measured during the transients (open symbols) are discarded before the analysis.

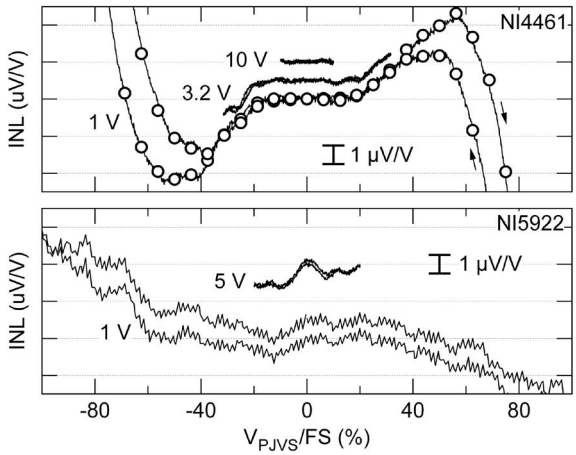


Fig. 7. (Top) INL of the NI4461 digitizer measured using the 1 V 0.48 Hz 64 (symbols) or 2048 (line) step per period triangular Josephson waveform. When the digitizer FS increases, a smaller fraction of the FS is investigated. (Bottom) INL of the NI5922 digitizer measured with the same signal but with 512 steps per period.

For NI5922, the settling time is below 5 $\mu$s, as stated in the specifications [15].

When a step voltage change is applied to the input of the digitizer, oscillations are observed before and after a voltage transition. These oscillations are an artifact of a digital filter implemented in the digitizers [15], [16]. The duration of these oscillations, that is a fixed number of samples, depends on the sampling frequency. For the NI4461, the delay is 63 samples. The amplitude of these oscillations increases with the amplitude of the voltage step applied to the input of the digitizer. A similar effect is observed on the digitizer NPL7767. In the NI5922, the digital filter can be selected among four different types. For the "8-tap Hanning" filter used for the data shown in Fig. 5, no oscillation is observed.

## VI. Integral Nonlinearity

One of the key parameters characterizing an ADC is the integral nonlinearity (INL). For this measurement, a triangular stepwise reference waveform, synthesized by the PJVS, is digitized by the unit under test (see Fig. 6). With the reference voltage being accurately known, the error, $\Delta V$, of the digitizer is directly given by the difference between the ADC's output and the Josephson voltage. For each step of a triangular stepwise signal, 50 samples are removed before and after the transition in order to avoid problems related to the oscillations described in the previous section. As explained in [11], the mean value of $\Delta V$ is then calculated from the remaining samples on the step. Ideally, $\Delta V$ should vary linearly with the reference Josephson voltage $V_{\mathrm{PJVS}}$. The INL is the deviation of $\Delta V$ from the ideal, normalized to the FSR.

Fig. 7 shows the INL of the NI4461 and NI5922 digitizers using a 1 V 0.48 Hz stepwise triangular Josephson waveform versus the reference voltage level normalized to the FS. For a larger FS, a smaller fraction of the input range of the digitizer is investigated by the 1 V signal. Changing the input range of the digitizer only affects the analog stage of the conversion chain amplifying the input signal to keep it in the range of the conversion stage of the digitizer. Since the shapes of the INL obtained with different input ranges are very similar, the observed INL is thus related to the conversion stage rather than to the analog input stage of the digitizer. This behavior is particulary clear for NI4461. This property suggests that the INL characterization of such digitizers does not need to be systematically repeated for every input range.

For NI4461, waveforms with 64 and 2048 steps per period have been used. Fig. 7 clearly shows that the INL does not depend on the number of steps present in the reference signal. INL measurements carried out using a waveform with a small number of steps per period are therefore still meaningful. This is particularly important since the number of steps per period that can be used for a waveform decreases necessarily at higher frequency. Due to the limited sampling frequency of the digitizer, the total number of sampled data per period of the reference signal decreases when frequency increases. Therefore, above a critical frequency, the number of sampled data remaining in each voltage step is very small for the calculation of the mean value of $\Delta V$.

Another interesting feature about the INL of NI4461 is a hysteresis that appears when the input signal is larger than 40% of the FS. NI5922 also presents a small hysteresis over its whole input range. The maximum hysteresis $H_m$ is defined by the largest difference between the INL values measured when the signal is ramping up and down at a given voltage.

The INL characterization has been repeated for the three digitizers using a waveform with 16 steps per period, an amplitude of 1 V, and for frequencies ranging from 0.48 Hz to 1 kHz. Fig. 8 shows the maximum INL observed as a function of the signal frequency, for different input ranges. Fig. 9 shows the maximum hysteresis, $H_m$, measured on the INL. Obviously, more information can be obtained when the input signal covers the whole input range of the digitizer i.e., on the 1 V FS input of NI4461 and NI5922. For NPL7767, the FS is fixed to 1.5 V. Therefore, the maximum signal of 1 V that our PJVS can actually generate covers only 66% of the input range.

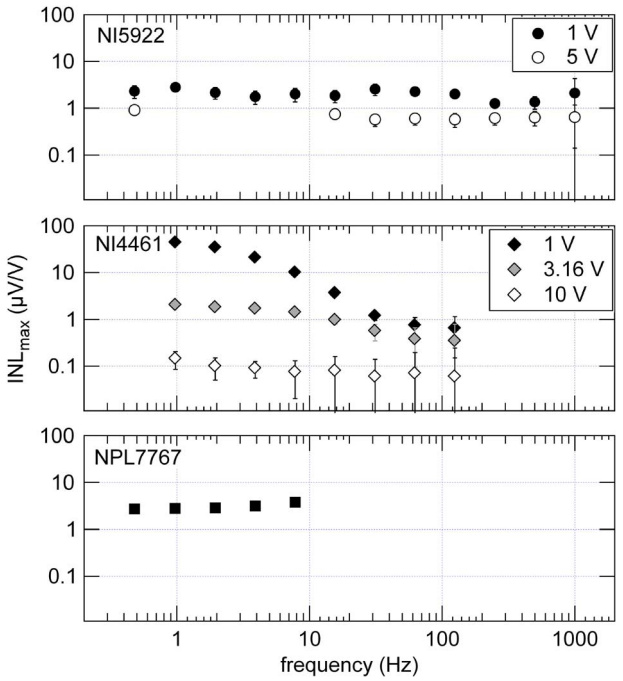


Fig. 8. Maximum INL of the three different digitizers measured using the 1 V 16 step per period triangular Josephson waveform at frequencies ranging from 0.48 Hz to 1 kHz. The different input ranges of the two NI digitizers have been investigated.

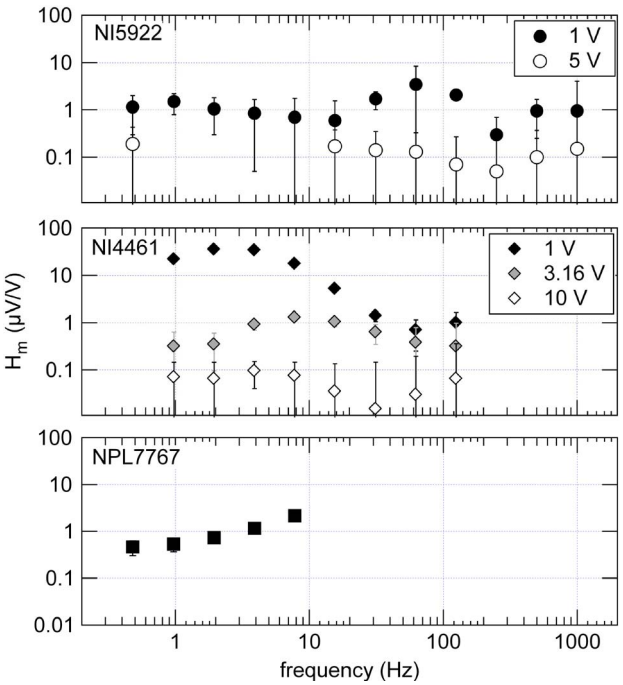


Fig. 9. Maximum hysteresis observed on the INL of the three different digitizers measured using the 1 V 16 step per period triangular Josephson waveform at frequencies ranging from 0.48 Hz to 1 kHz.

For the NI4461 digitizer, the maximum INL is more than 80 $\mu$V/V at low frequencies and decreases below 1 $\mu$V/V at frequencies higher than 40 Hz. In addition, a large hysteresis is present at low frequencies and dramatically decreases as frequency increases. Such a behavior is more than likely related to thermal effects. If a large signal ($> 40\%$ of FS) is applied to the input of the digitizer for a while, local temperature within the electronic circuit certainly increases. The behavior of the neighboring components is then disturbed: a large INL and a hysteresis are then observed. If the large input signal is applied to the digitizer for a "short" time (less than a few milliseconds), a temperature rise is limited and has a reduced impact on the circuit behavior.

Such a behavior is not visible for the NI5922 digitizer. Even if a small increase in the hysteresis appears around 60 Hz, neither the INL nor the hysteresis exceeds 3 or 4 $\mu$V/V over the whole frequency range tested.

For NPL7767, the INL remains roughly stable below 4 $\mu$V/V, whereas the hysteresis increases more than four times between 0.48 and 7.8 Hz.

The maximum frequency tested is not the same for every digitizer. The limitation does not come from the PJVS itself because the rising time of our system is about 800 ns. The limiting factor is in fact the sampling frequency of the digitizer. Indeed, the time elapsed on each step decreases when the signal frequency increases. Therefore, for a given sampling frequency, the number of sampled point on each step becomes very small when the signal frequency increases above a certain limit.

## VII. Conclusion

One of the limitations in the characterization of high-resolution digitizers is the lack of accuracy of the source used to generate the reference input signal. The use of a PJVS can, to some extent, solve this problem.

To this end, a test bench has been developed for the systematic characterization of metrological grade ADCs. The reference signal is either a dc voltage or a stepwise waveform generated by the PJVS. The difference between low noise, accurate Josephson voltage and the reading of the digitizer yields directly the error of the converter.

Three different digitizers have been characterized in terms of noise (i.e., the Allan deviation) and INL. None of the digitizers outperforms the others on every tested parameter. NPL7767 shows the smallest $1/f$ noise floor ($< 100$ nV/V) at 1 V, whereas NI5922 is better in terms of white noise ($< 2$ nV/V/$\sqrt{\text{Hz}}$). The INL of NI4461 is smaller than 1 $\mu$V/V at frequencies higher than 40 Hz, but large INL and a significant hysteresis appear at lower frequencies. The INL and the hysteresis of NI5922 remain below 4 $\mu$V/V for frequencies ranging from 0.5 Hz to 1 kHz.

Clearly, a tradeoff between different parameters has to be made during the design of a new ADC-based application. Therefore, the use of such a test bench for the characterization of high-performance digitizers can provide precious information for the selection of the most suitable digitizer in a particular application.

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## REFERENCES


[1] F. Overney and B. Jeanneret, "Realization of an inductance scale traceable to the quantum Hall effect using an automated synchronous sampling system," *Metrologia*, vol. 47, no. 6, pp. 690–698, Dec. 2010.

[2] B. Jeanneret, F. Overney, A. Rüfenacht, and J. Nissilä, "Strong attenuation of the transients effect in square waves synthesized with a programmable Josephson voltage standard," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 7, pp. 1894–1899, Jul. 2010.

[3] A. Rüfenacht, F. Overney, A. Mortara, and B. Jeanneret, "Thermal transfer standard validation of the Josephson-voltage-standard-locked sine wave synthesizer," *IEEE Trans. Instrum. Meas.*, 2011, submitted for publication.

[4] L. Palafox, G. Ramm, R. Behr, W. G. K. Ihlenfeld, and H. Moser, "Primary AC power standard based on programmable Josephson junction arrays," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 2, pp. 534–537, Apr. 2007.

[5] B. C. Waltrip, B. Gong, T. L. Nelson, Y. Wang, C. J. Burroughs, A. Rüfenacht, S. Benz, and P. Dresselhaus, "AC power standard using a programmable Josephson voltage standard," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 1041–1048, Apr. 2009.

[6] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, IEEE Std. 1241-2000, 2000.

[7] *IEEE Standard for Digitizing Waveform Recorders*, IEEE Std. 1057-2007, 2007.

[8] B. Jeanneret and S. Benz, "Application of the Josephson effect in electrical metrology," *Eur. Phys. J. B*, vol. 172, no. 1, pp. 181–206, Jun. 2009.

[9] W. G. K. Ihlenfeld, E. Mohns, R. Behr, J. Williams, P. Patel, G. Ramm, and H. Bachmair, "Characterization of a high resolution analog-to-digital converter with a Josephson AC voltage source," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 649–652, Apr. 2005.

[10] R. Iuzzolino, L. Palafox, W. G. K. Ihlenfeld, E. Mohns, and C. Brendel, "Design and characterization of a sampling system based on $\Sigma$–$\Delta$ analog-to-digital converters for electrical metrology," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 786–790, Apr. 2009.

[11] F. Overney, A. Rüfenacht, P.-P. Braun, and B. Jeanneret, "Josephson-based test bench for ac characterization of analog-to-digital converters," in *Proc. CPEM Dig.*, 2010, pp. 215–216.

[12] H. E. van den Brom, E. Houtzager, Q. E. Martina, and G. Rietveld, "Calibrating a sampling voltmeter using a binary Josephson system," in *Proc. CPEM Dig.*, 2008, pp. 100–101.

[13] B. Jeanneret, F. Overney, L. Callegaro, A. Mortara, and A. Rüfenacht, "Josephson-voltage-standard-locked sine wave synthesizer: Margin evaluation and stability," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 791–796, Apr. 2009.

[14] K. Mueller, R. Behr, T. Weimann, L. Palafox, D. Olaya, P. Dresselhaus, and S. Benz, "1 V and 10 V SNS programmable voltage standards for 70 GHz," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 981–986, Jun. 2009.

[15] NI PXI/PCI-5922 Specifications, 2007. [Online]. Available: http://www.ni.com/pdf/manuals/374049c.pdf

[16] NI-PXI 4461 Specifications, 2008. [Online]. Available: http://www.ni.com/pdf/manuals/373770j.pdf

[17] AD7767 specification. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD7767.pdf

[18] P. S. Wright and P. Clarkson, "Development of an ethernet enabled digitizer for on-site ac measurements," in *Proc. CPEM Dig.*, 2010, pp. 245–246.


**Frédéric Overney** (M'07) was born in Yverdon, Switzerland, in 1967. He received the E.T.S. degree in microtechnics from the School of Business and Engineering Vaud (HEIG-VD),Yverdon, in 1990 and the M.S. degree in physics from Swiss Federal Institute of Technology, Zurich, Switzerland, in 1995.

Then, he joined the Federal Office of Metrology (METAS), Bern-Wabern, Switzerland, where he extended measurement capabilities in the field of alternating/direct-current transfer up to 1000 V and participated in the development of a new time-and-frequency transfer method based on geodetic global positioning system receivers. His current research interests include precision measurements of impedance and the development of measuring systems for electrical quantities.

**Alain Rüfenacht** was born in La Chaux-de-Fonds, Switzerland, in 1975. He received the Ph.D. degree from the University of de Neuchâtel, Neuchâtel, Switzerland, in 2005, for his work in collaboration with IBM Zurich Research Laboratory, Ruschlikon, Switzerland, on high-temperature superconducting ultrathin films.

In 1999, he was a Scientific Collaborator with the Electrical Quantum Standards Laboratory, Federal Office of Metrology (METAS), Bern-Wabern, Switzerland. In 2007 and 2008, he was a Guest Researcher with the Quantum Voltage Project, National Institute of Standards and Technology, Boulder, CO, focusing mainly on the integration of Josephson junction arrays into voltage standards. Since 2009, he has been with METAS, working on the capacitance standard charged with single-electron pumps and Josephson voltage standards.

**Jean-Pierre Braun** (M'92) obtained the B.E. degree from the Ecole d'Ingénieurs de Genève, Geneva, Switzerland, in 1980; the M.E.M degree from the University of Technology Sydney, Sydney, Australia, in 1993; and the M.Eng.Sc. degree from the University of New South Wales, Sydney, in 2000.

In 2007, he joined the Power and Energy Laboratory, Federal Office of Metrology (METAS), Bern-Wabern, Switzerland, as a Scientific Collaborator. He has over twenty five years of experience in product development and has held positions such as a Hardware Design Engineer, a Systems Engineer, and a Group Manager. His current research interests include the field of power quality and signal processing.

**Blaise Jeanneret** was born in Fleurier, Switzerland, in 1959. He received the Ph.D. degree in experimental condensed matter physics from the University of Neuchâtel, Neuchâtel, Switzerland, in 1989.

In 1990 and 1991, he was a Guest Scientist with National Institute of Standards and Technology, Boulder, CO, working on the so-called high-temperature superconductors. In 1992, he returned to the University of Neuchâtel. In 1993, he was with the Institute for Micro- and Optoelectronics, Swiss Federal Institute of Technology (EPFL), Zurich, Switzerland, where he was involved in the research on the quantum Hall effect. Since 1996, he has been with the Federal Office of Metrology (METAS), Bern-Wabern, Switzerland, where he was engaged in the work on the quantum Hall effect. In 1997, he became the Head of the Quantum Metrology Laboratory, METAS. His research interests include electrical quantum metrology.

**Paul S. Wright** was born in Twickenham, U.K., in 1962. He received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from the University of Surrey, Surrey, U.K.

He spent three years as a Research Fellow with the University of Surrey, working in the field of spacecraft sensors and attitude control. This was followed by three years with Central Electricity Research Laboratory, Surrey, where he worked on advanced control systems. In 1992, he was with the National Physical Laboratory, Teddington, where he is a Principle Research Scientist specializing in alternating-current (ac) measurements and waveform analysis. His current research interests include ac power standards, ac/direct-current transfer measurements, digital sampling systems, and the analysis of nonsinusoidal/nonstationary waveforms applied to power quality measurements and SmartGrid development.

Dr. Wright is a Chartered Engineer and a member of the Institution of Electrical Engineers.