Errata

- **Universal Synchronous Asynchronous Receiver Transmitter (USART)**
  - **Hardware Handshake (21)**
- **Serial Peripheral Interface (SPI)**
  - **Pulse Generation on SPCK (20)**
  - **MCK/32 Clock Selection (19)**
- **Parallel Input/Output Controller (PIO)**
  - **Leakage on PA17 - PA20 (18)**
  - **Electrical Characteristics on NRST and PA0-PA16 (17)**
  - **Drive Low NRST and PA0-PA16 (16)**
- **PLL**
  - **Maximum Output Frequency (15)**
- **Two Wire Interfere (TWI)**
  - **Clock Divider (14)**
  - **Behavior of OVRE Bit (22)**
- **Serial Synchronous Controller (SSC)**
  - **Transmitter Limitations in Slave Mode (13)**
  - **Periodic Transmission Limitations in Master Mode (12)**
- **Voltage Regulator**
  - **Load Versus Temperature (8)**
  - **Current Consumption in Deep Mode (7)**
- **Pulse Width Modulation Controller (PWM)**
  - **Update when PWM_CCNTx = 0 or 1 (11)**
  - **Update when PWM_CPRDx = 0 (10)**
  - **Counter Start Value (9)**
  - **Constraints on Duty Cycle (6)**
  - **Behavior of CHIDx Status Bits in the PWM_SR Register (5)**
- **Non Volatile Memory Bits (NVM)**
  - **NVM Write/Erase Cycles Number (4)**
- **Memory Controller (MC)**
  - **Address Decoder (3)**
  - **Abort Source Bits do not Clear (2)**
- **Power Management Controller (PMC)**
  - **Constraints on Master Clock Selection Sequence (1)**

This Errata Sheet refers to:

AT91SAM7S64 (revision G) devices packaged in 64-lead LQFP with the marking AT91SAM7S64-AU-001 and the product number marked in the bottom left-hand corner of the package being 58814G.

ARM7TDMI®-based Microcontroller

AT91SAM7S64

Errata Sheet

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22. TWI: Behavior of OVRE Bit

In Master Mode during a read access, if the sequence described as follows occurs;

1. A byte is received but not read through the TWI_RHR.
2. A step command is performed through the TWI_CR to end the read access.
3. The last data byte is received.

The Overrun Flag (OVRE) does not rise, whereas a data byte has been lost:

Problem Fix/Workaround

None.

21. USART: Hardware Handshake

The Hardware Handshake does not work at speeds higher than 750 kbauds.

Problem Fix/Workaround

None.

20. SPI: Pulse Generation on SPCK

In Master Mode, there is an additional pulse generated on SPCK when the SPI is configured as follows:

- The Baudrate is odd and different from 1
- The Polarity is set to 1
- The Phase is set to 0

Problem Fix/Workaround

None.

19. SPI: MCK/32 Clock Selection

When the selected clock is MCK/32 (FDIV = 1), data is properly transferred in both directions but the RDRF flag is set too soon and a first read attempt does not reset it. OVRES flag is therefore erroneously raised.

When the selected clock is MCK/32 (FDIV = 1), PDC pointers are not correctly incremented.

Problem Fix/Workaround

Use FDIV = 0.

18. PIO: Leakage on PA17 - PA20

When PA17, PA18, PA19 or PA20 (the I/O lines multiplexed with the analog inputs) are set as digital inputs with pull-up disabled, the leakage can be 5 µA in worst case and 90 nA in typical case per I/O when the I/O is set externally at low level.

Problem Fix/Workaround

Set the I/O to VDDIO by internal or external pull-up.

17. PIO: Electrical Characteristics on NRST and PA0-PA16 and PA21-31

When NRST or PA0-PA16 or PA21-PA31 are set as digital inputs with pull-up enabled, the voltage of the I/O stabilizes at VPull-up.

Vpull-up

VPull-up Min	VPull-up Max
VDDIO - 0.65 V	VDDIO - 0.45 V

This condition causes a leakage through VDDIO. This leakage is 45 µA per pad in worst case at 3.3 V and 25 µA at 1.8V.

I Leakage

Parameter	Typ	Max
I Leakage at 3,3V	2.5 µA	45 µA
I Leakage at 1.8V	1 µA	25 µA

Problem Fix/Workaround

It is recommended to use an external pull-up if needed.

16. PIO: Drive Low NRST, PA0-PA16 and PA21-PA31

When NRST or PA0-PA16 and or PA21-PA31 are set as digital inputs with pull-up enabled, driving the I/O with an output impedance higher than 500 ohms may not drive the I/O to a logical zero.

Problem Fix/Workaround

Output impedance must be lower than 500 ohms.

15. PLL: Maximum output frequency

The maximum output frequency delivered by the PLL is 200 MHz.

Problem Fix/Workaround

The output frequency of the PLL must be lower than 200 MHz.

14. TWI: Clock divider

The value of CLDIV x 2^{CKDIV} must be less than or equal to 8191, the value of CHDIV x 2^{CKDIV} must be less than or equal to 8191·

Problem Fix/Workaround

None.

13. SSC: Transmitter Limitations in Slave Mode

If TK is programmed as an input and TF is programmed as an output and requested to be set to low/high during data emission, the Frame Synchro signal is generated one bit clock period after the data start and one data bit is lost. This problem does not exist when generating a periodic Frame Synchro signal.

If TK is programmed as an output and TF is programmed as an input, it is impossible to emit data when the start (rising or falling) edge of the Frame Synchro signal has a start delay equal to zero.

Problem Fix/Workaround

None.

12. SSC: Periodic Transmission Limitations in Master Mode

If the Least Significant Bit is sent first (MSBF = 0), the first TAG during the frame synchro is not sent.

Problem Fix/Workaround

None.

11. PWM: Update when PWM_CCNTx = 0 or 1

If the Channel Counter Register value is 0 or 1, the Channel Period Register or Channel Duty Cycle Register is directly modified when writing the Channel Update Register.

Problem Fix/Workaround

Check the Channel Counter Register before writing the update register.

10. PWM: Update when PWM_CPRDx = 0

When Channel Period Register equals 0, the period update is not operational.

Problem Fix/Workaround

Do not write 0 in the period register.

9. PWM: Counter Start Value

In left aligned mode, the first start value of the counter is 0. For the other periods, the counter starts at 1.

Problem Fix/Workaround

None.

8. Voltage Regulator: Current Consumption in Deep Mode

Current consumption in Deep Mode is maximum 60 µA instead of 25 µA.

Due to current rejection from VDDIN to VDDCORE, the current consumption in Deep Mode cannot be guaranteed. Instead, 60 µA is guaranteed whatever the condition.

Problem Fix/Workaround

None.

7. Voltage Regulator: Load Versus Temperature

Maximum load is 50 mA at 85 °C (instead of 100 mA).

Maximum load is 100 mA at 70°C.

Problem Fix/Workaround

None.

6. PWM: Constraints on Duty Cycle Value

A value of 0 is forbidden in the Channel Duty Cycle Register (PWM_CDTYx)

Problem Fix/Workaround

0 corresponds to a permanent high or low signal. The PIO controller may ensure this level when needed by disabling PWM, and using the corresponding I/O as an output with a value 0 or 1.

5. PWM: Behavior of CHIDx Status Bits in the PWM_SR Register

Erratic behavior of the CHIDx status bit in the PWM_SR Register. When a channel is disabled by writing in the PWM_DIS Register just after enabling it (before completion of a Clock Period of the clock selected for the channel), the PWM line is internally disabled but the CHIDx status bit in the PWM_SR stays at 1.

Problem Fix/Workaround

Do not disable a channel before completion of one period of the selected clock.

4. NVM Bits: Write/Erase Cycles Number

The maximum number of write/erase cycles for Non Volatile Memory bits is 100. This includes Lock Bits (LOCKx), General Purpose NVM bits (GPNVMx) and the Security Bit.

Not applicable to 64 KB Flash memory.

Problem Fix/Workaround

None.

3.MC: Address Decoder:

If an access (data read, data write or prefetch) is done in the address area 0x0030 0000 to 0x003F FFFF, no abort is generated.

Problem Fix/Workaround

None.

2. MC: Abort Source Bits Do Not Clear

In the MC_ASR register of the Memory Controller: MST0, MST1, SVMST0 and SVMST1 status bits are not cleared after the MC_ASR register is read.

Problem Fix/Workaround

None.

1. PMC: Constraints on the Master Clock Selection Sequence

The PMC_MCKR register must not be programmed in a single write operation.

Problem Fix/Workaround

The preferred programming sequence for the PMC_MCKR register is as follows:

If a new value for CSS field corresponds to PLL Clock,

- Program the PRES field in the PMC_MCKR.
- Wait for the MCKRDY bit to be set in the PMC_SR register.
- Program the CSS field in the PMC_MCKR.
- Wait for the MCKRDY bit to be set in the PMC_SR register.

If a new value for CSS field corresponds to Main Clock or Slow Clock,

- Program the CSS field in the PMC_MCKR.
- Wait for the MCKRDY bit to be set in the PMC_SR register.
- Program the PRES field in the PMC_MCKR.
- Wait for the MCKRDY bit to be set in the PMC_SR register.

Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6099A	15-Apr-05	First issue. Qualified on web	
6099B	06-jun-05	Errata added: to PWM, Errata given for SSC, TWI, PLL, PIO, SPI	CSR 05-326

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6099B–ATARM–20-Jun-05