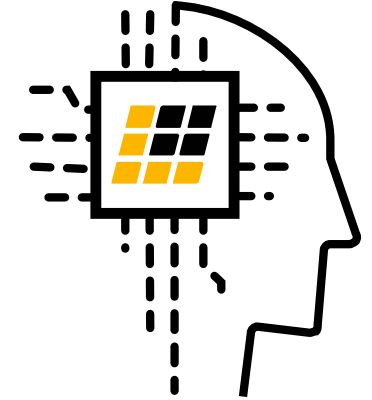
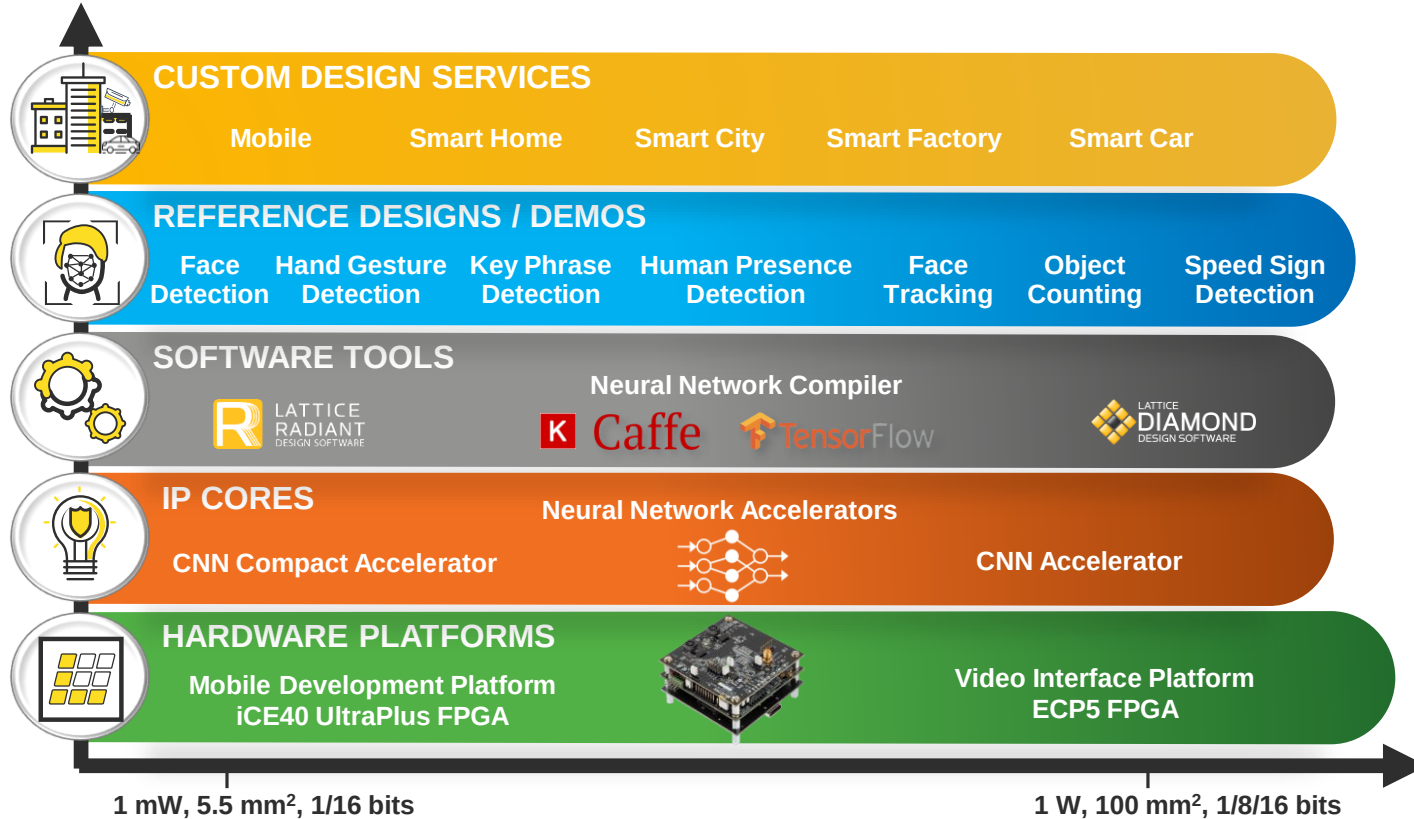


# Lattice sensAI

*Complete Machine Learning Solution*



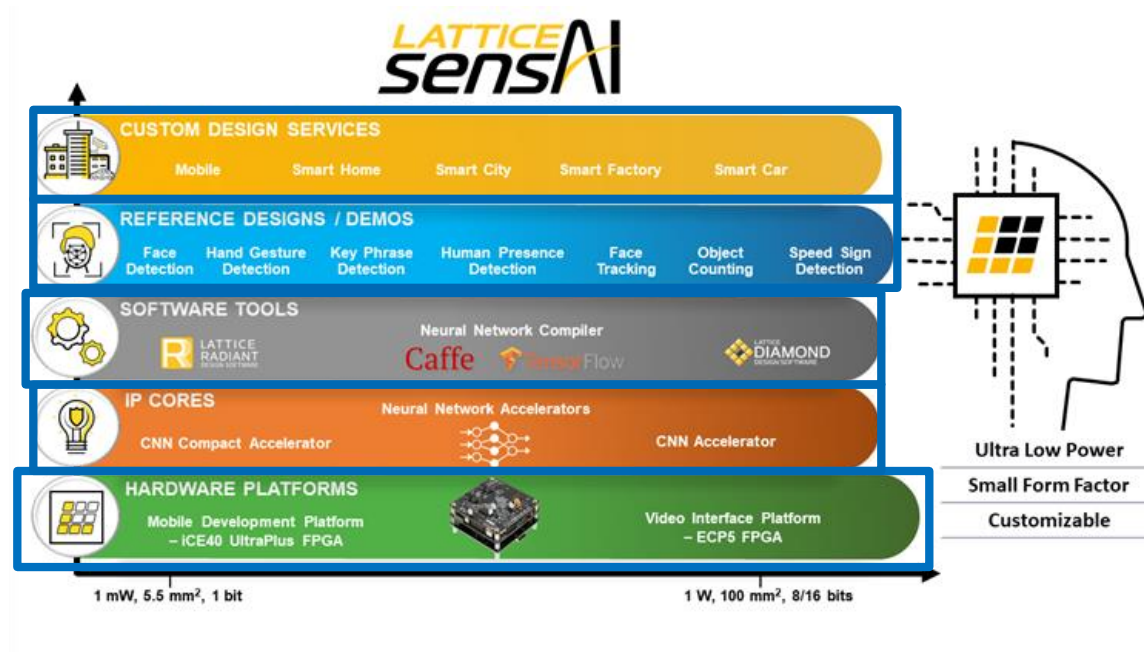
Ultra Low Power

Small Form Factor

Customizable

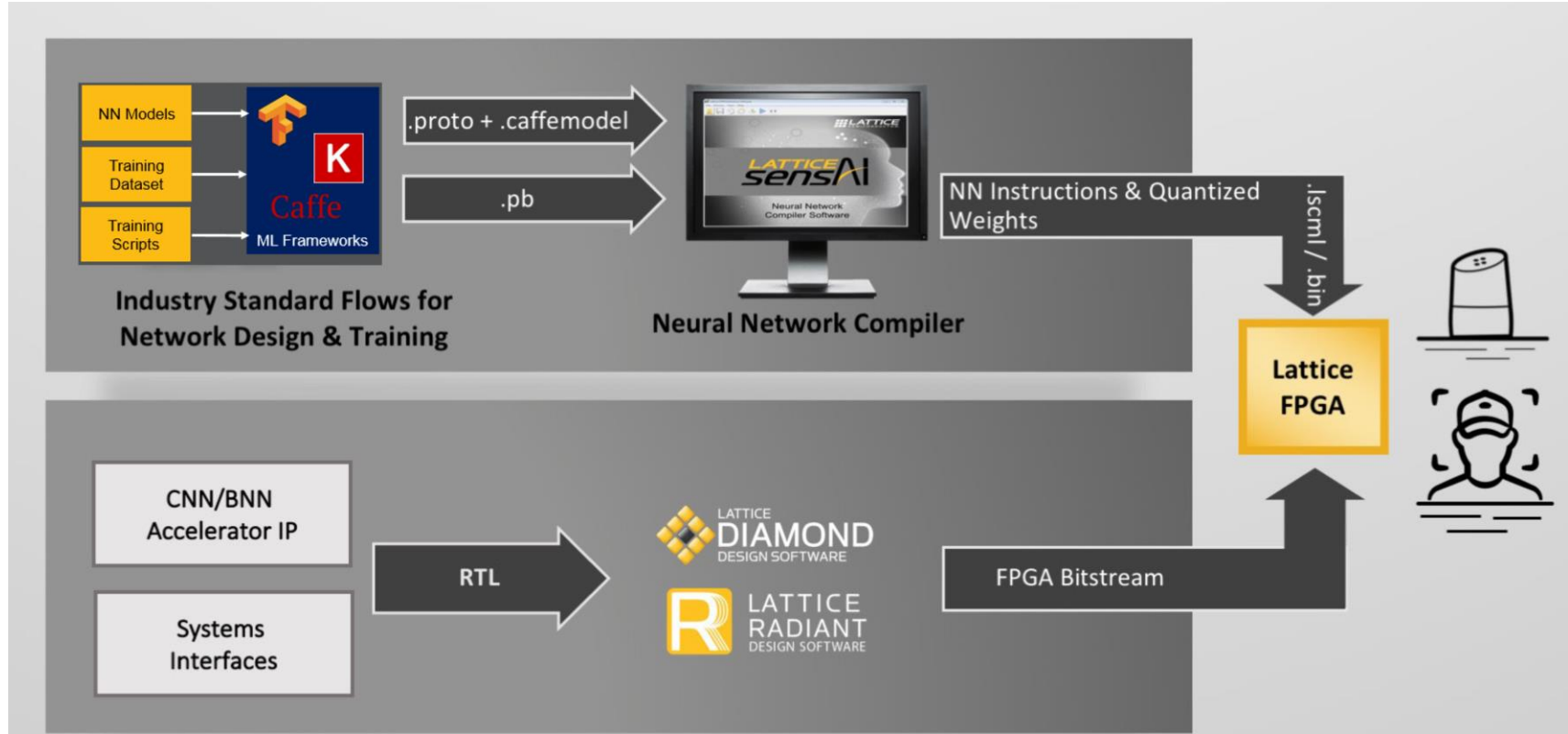
# Overview

- Lattice sensAI is our entire Machine Learning Solution stack



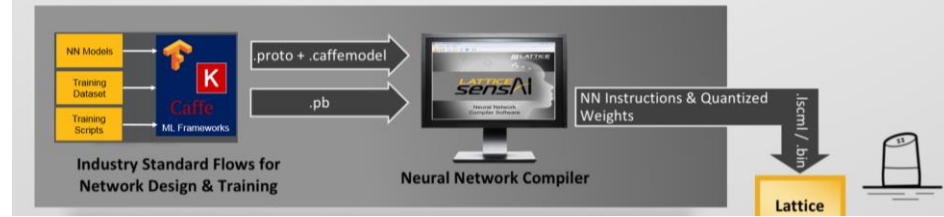
# Design Methodology

## Overview



# Design Flow

## The NN Side...



- Lattice NN Compiler converts TensorFlow/Caffe output into a binary format to be used by Lattice CNN IP.
  - Includes floating point to fixed point conversion + adjustment of coefficient size (bit width).
- Output is a binary file containing a sequence of commands that are interpreted by Lattice CNN IP
- FPGA resource information such as size and number of available EBRs, number of DSPs and overall LUT count are considered.

# Design Flow

The FPGA side...

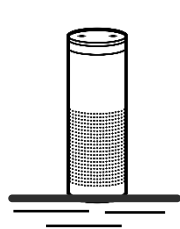
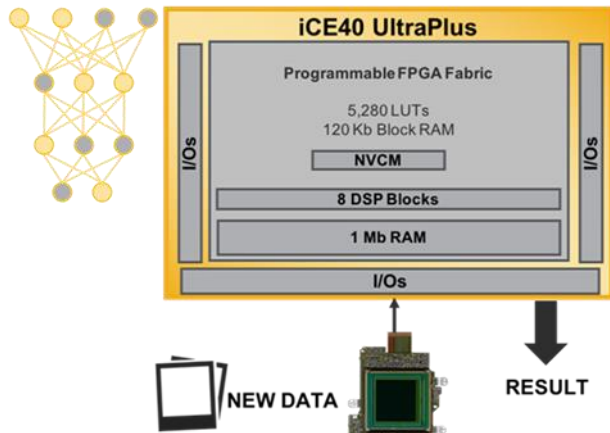


- Lattice CNN IP is optimized for common operations of Neural Network.
- Pre-mapped into Lattice FPGA architecture
  - Identical for all NN implementations
- Output from Lattice NN Compiler is used by the CNN IP to execute the Neural Network and generate a result.

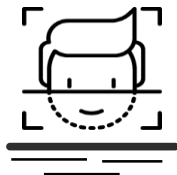
# Reference Designs/Demos

Optimized for Ultra-Low Power Consumption

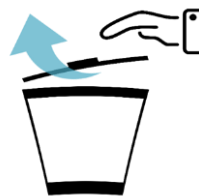
<1-10 mWs



Key Phrase  
Detection



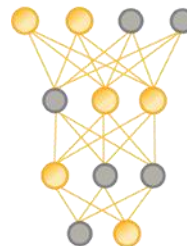
Face/Object  
Detection



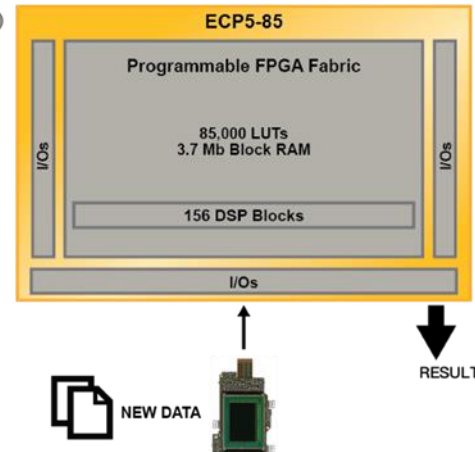
Hand Gesture  
Detection



Human Presence  
Detection



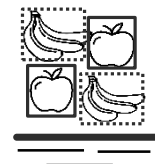
<1 W



Face/Object  
Tracking



Speed Sign  
Detection



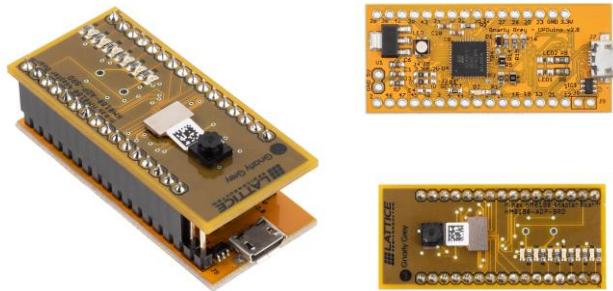
Object  
Counting



# Hardware Platforms

## Modular Platforms for Rapid Prototyping

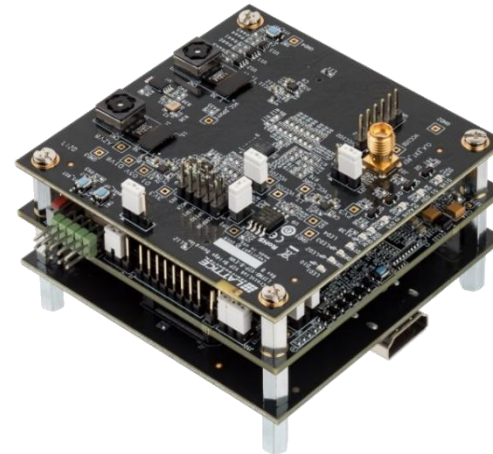
### Himax HM01B0 UPduino Shield Board



#### Key features

- Vision and Audio sensors
- Compact 22x50 mm
- Himax HM01B0 sensor board
- Upduino form factor UltraPlus board

### Video Interface Platform (VIP)



China Electronics Market  
2017 Editor Choice Award

#### Key features

- ECP5 FPGA consuming under 1W of power consumption
- Flexible video connectivity with support for MIPI CSI-2, eDP, HDMI, GigE Vision, USB 3.0, and more



# New in sensAI 2.0

|                   |                                                                                      |
|-------------------|--------------------------------------------------------------------------------------|
| Quick Start Guide | ECP5 Object Counting Quick Start Guide                                               |
|                   | iCE40 UltraPlus Human Presence Detect Quick Start Guide                              |
|                   |                                                                                      |
| Demos             | EVDK Human Counting Demonstration Bitstream & Binary file                            |
|                   | EVDK Human Counting Demonstration User Guide                                         |
|                   | HM01B0 UPduino Shield Human Presence Detection Bitstream & Binary file               |
|                   | HM01B0 UPduino Shield Human Presence Detection User Guide                            |
|                   |                                                                                      |
| RDs               | Object Counting Using CNN Accelerator IP – RD Documentation                          |
|                   | Object Counting Using CNN Accelerator IP – RD Project Files                          |
|                   | Human Presence Detection Using Compact CNN IP – RD Project Files                     |
|                   | Human Presence Detection Using Compact CNN IP – RD Documentation                     |
|                   |                                                                                      |
| NN & Training     | ECP5 Human Counting Sample Image Data, NN, Python Training scripts                   |
|                   | iCE40 UltraPlus Human Presence Detect Sample Image Data, NN, Python Training scripts |

# Production Quality Reference Designs

## Human Counting on ECP5

- ECP5-85 (Embedded Vision Kit)
- Detects and count number of people in a frame
  - Body can be as small as 6 pixels
  - Can detect a person up to 25 ft from HW at different orientations
  - Training dataset and input files to ML Frameworks are included.

# Production Quality Reference Designs



# Production Quality Reference Designs

Human Presence Detection on iCE40 UltraPlus

- iCE40 UltraPlus 5K on Himax UPduino Shield
- Detects presence of a human
  - Body can be as small as 10-15% of the frame
  - Can detect a person up to 15 ft from HW
  - Training dataset and input files to ML Frameworks are included.

# SensAI on Lattice Website

Home page banner

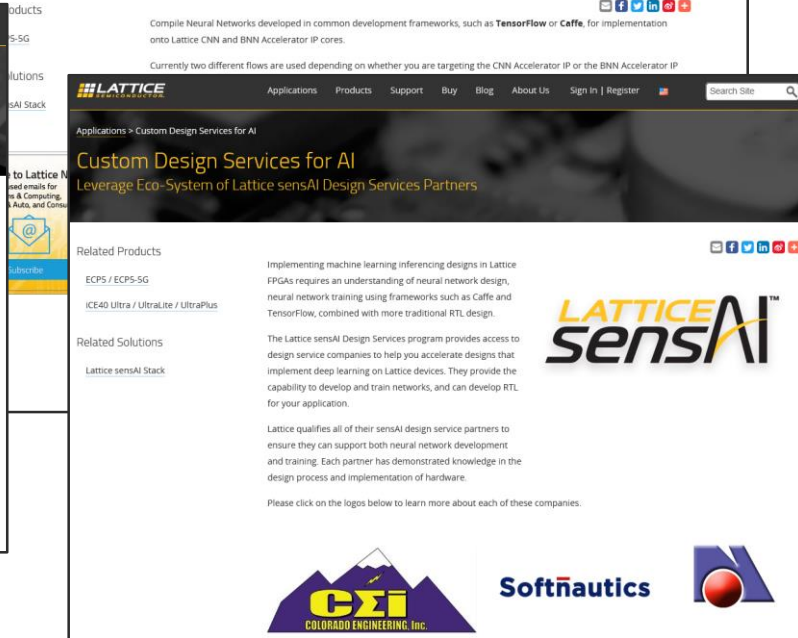
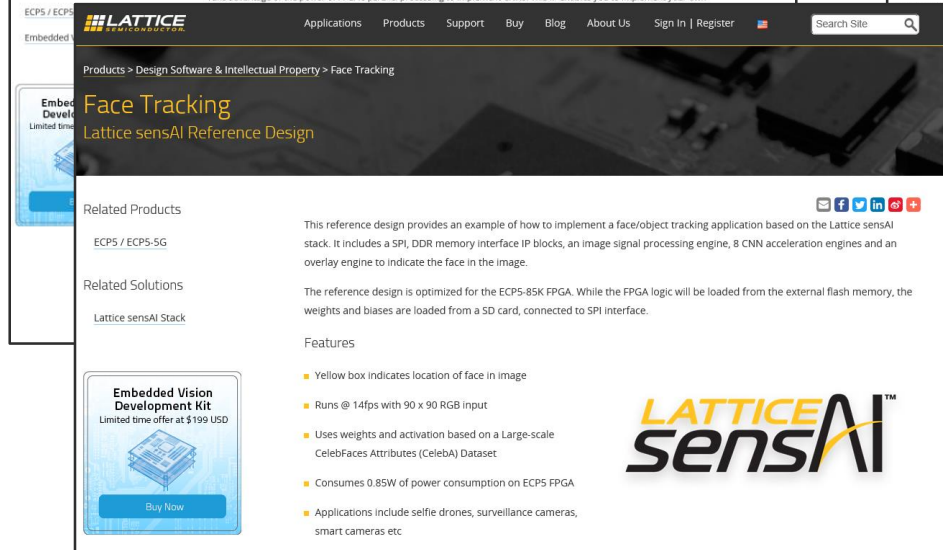


AI landing page

The landing page has a dark header with the Lattice Semiconductor logo and navigation links: Applications, Products, Support, Buy, Blog, About Us, Sign In | Register. A search bar is on the right. Below the header, the page title is 'Lattice sensAI Stack' with the subtitle 'Accelerate Integration of Flexible Inferencing at the Edge'. The 'Related Products' section lists 'ECPS / ECPS-5G' and 'ICE40 Ultra / UltraLite / UltraPlus'. The 'Related Solutions' section lists 'Video Interface Platform' and 'Embedded Vision Solutions'. A central text block describes the full-featured Lattice sensAI stack, including modular hardware platforms, neural network IP cores, software tools, reference designs, and custom design services. It highlights flexible inferencing solutions optimized for power consumption from under 1mW-1W and package sizes starting at 5.5mm<sup>2</sup>. The 'Related Products' section also includes an 'Embedded Vision Development Kit' with a 'Buy Now' button. The bottom section is a detailed diagram of the Lattice sensAI stack, organized into five horizontal layers: CUSTOM DESIGN SERVICES (Mobile, Smart Home, Smart City, Smart Factory, Smart Car), REFERENCE DESIGNS / DEMOS (Face Detection, Key Phrase Detection, Face Tracking, Object Counting, Speed Sign Detection), SOFTWARE TOOLS (Lattice SDK, Neural Network Compiler, Caffe, TensorFlow, DIAMOND), IP CORES (Blink Accelerator, Neural Network Accelerators, CNN Accelerator), and HARDWARE PLATFORMS (Mobile Development Platform - UltraPlus FPGAs, Video Interface Platform - ECPS FPGAs). A vertical bar on the right side of the diagram lists the benefits: Ultra Low Power, Small Form Factor, Customizable, and Production Priced. At the bottom, two performance metrics are shown: '1mW, 5.5mm<sup>2</sup>, 1 bit, ~\$1' and '1W, 100mm<sup>2</sup>, 8/16 bits, ~\$10'.

# SensAI on Lattice Website

~20 new web pages and technical documents





# SensAI on Lattice Website

## Product brochure

### Ultra-Low Power Lattice sensAI™ Stack

Accelerate Integration of Flexible Inferencing at the Edge

With solutions optimized for ultra-low power consumption (under 1 mW-1 W), small package footprints (MPN CSI-2, LVDS, Gige, etc.), and high-volume pricing (~\$1-\$10), the Lattice sensAI stack computing close to the source of data.

**Custom Design Services**

**REFERENCE DESIGNS / DEMOS**

**SOFTWARE TOOLS**

**IP CORES**

**HARDWARE PLATFORMS**

Complete technology stack for ultra low power flexible inferencing

### Lattice sensAI Hardware Platforms

- Mobile Development Platform (MDP)**
  - Key Features
    - ICE40 UltraPlus™ FPGA consuming low mW of power consumption
    - Includes image sensor, microphones, compass/pressure/gyro sensors, etc.
- Video Interface Platform (VIP)**
  - Key Features
    - ECPS™ FPGA consuming under 1W of power consumption
    - Supports MPN CSI-2, xDP, HDMI, Gige Vision, USB 3, etc.

### Lattice sensAI IP Cores

| IP Core         | OPN          | Key Features                                            |
|-----------------|--------------|---------------------------------------------------------|
| MPN Accelerator | NA           | Optimized for ICE40 UltraPlus FPGA                      |
| CMN Accelerator | CMNACCEL-ESU | Optimized for ECPS FPGA, supports variable quantization |

### Lattice sensAI Software Tools

| Software Tool           | Key Features                                                    |
|-------------------------|-----------------------------------------------------------------|
| Neural Network Compiler | Supports Caffe and TensorFlow. No prior RTL experience required |

### Lattice sensAI Reference Designs and Demos

| Reference Design/Demos | Supported FPGA / HW Platform                                 | Power Consumption |
|------------------------|--------------------------------------------------------------|-------------------|
| Face Detection         | ICE40 UltraPlus, ICE40 UltraPlus Mobile Development Platform | < 1mW             |
| Key Phrase Detection   | ICE40 UltraPlus, ICE40 UltraPlus Mobile Development Platform | < 5mW             |
| Face Tracking          | ECPS, Video Interface Platform                               | < 1W              |
| Object Counting        | ECPS, Video Interface Platform                               | < 1W              |
| Speed Sign Detection   | ECPS, Video Interface Platform                               | < 1W              |

### Lattice sensAI Stack Custom Design Services

Have custom AI solution needs? The sensAI stack includes an ecosystem of select, global design service partners that can deliver custom solutions for a range of end-applications, including mobile, smart home, smart city, smart factory, and smart cars. Please contact your local sales representative to request more information.

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April 2018  
000001-0001-0001

[www.latticesemi.com/sensAI](http://www.latticesemi.com/sensAI)

## White paper



### Accelerating Implementation of Low Power Artificial Intelligence at the Edge

A Lattice Semiconductor White Paper  
May 2018

The emergence of smart factories, cities, homes and mobile are driving shifts in systems architectures and new applications that require increased intelligence at the edge. Artificial Intelligence/Machine Learning silicon solutions are essential to meeting the requirements for this new generation of AI-based edge computing applications.

Designers building computing solutions on the edge are challenged to meet new requirements for flexibility, low power, small form factor and low cost, without compromising performance and in hotly competitive market conditions. Systems that integrate low power inferencing close to the source of IoT data utilizing lower density FPGAs optimized for low power operation, can meet the stringent performance and power limitations imposed on the network edge with a time to market advantage.

The new Lattice sensAI™ stack, a comprehensive developmental ecosystem, simplifies the task of building flexible inferencing solutions optimized for the edge. With variety of IP, tools, reference designs, and design expertise developers can utilize the ecosystem to get to market quickly with innovative solutions.

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Accelerating Implementation of Low Power Artificial Intelligence at the Edge  
WP-0014





# Summary

- Lattice sensAI accelerates integration of always-on, on-device AI in Edge IoT devices
  - Ultra low-power solutions: 1mW-1W
  - Small size packages: 5.5mm<sup>2</sup>- 100mm<sup>2</sup>
  - Variable quantization: 1, 8, and 16 bits
  - Flexibility and Scalability
    - Seamless integration into existing designs with flexible interface support
    - Rapid design space exploration for power-performance-accuracy tradeoffs
    - Reprogrammable to support updated trained models and evolving algorithms
- Get started today with complete technology stack offerings!

# Collateral Review & Demo

# Quick Start PDF

# Quick Start Guide Walk Through

## FPGA ML/AI Design Process

- Setting up the basic environment
- Preparing the dataset
- Training the Machine
- Creating the frozen file (\*.pb)
- Creating the binary file with Lattice sensAI™ 2.0 program
- Programming the binary and bitstream files to VIP board and SD card



## ECP5 Object Counting Quick Start Guide

*Internal Review*

### Application Note

FPGA-AN-02006-1.0

May 2019

# Demo Steps

- Explain the Training & NN implementation
  - Typically in Linux system
- Start with .PB file and run it through NN Compiler to generate binary file
- Open RD design project and explain FPGA design
  - FPGA bitstream generated
- HW demo