MICROCHIP MASTERs 2019

23110 SIG1

Electromagnetic Compatibility (EMC) Demystified

SMART | CONNECTED | SECURE

MICROCHIP

Agenda

- What is ‘EMC’ and Why We Care About It
- Characteristics and Measurement of Electrical Noise
- Noise Path Control
- Signal Integrity
- Design for EMC
  - Circuit Design for EMC
  - PCB Design for EMC
- Real-Life EMC ‘uh-ohs’!
- EMC Guideline Summary

Class Objectives

When you walk out of this class you will….

- **Have an Appreciation of What EMC Means and Why it Matters**
- **Understand How to Approach**
  - Design for EMC
  - Solving existing EMC issues
- **Be Able to Apply System and PCB Design Techniques for EMC**
- **Know Where to Look for Additional Information and Guidance**

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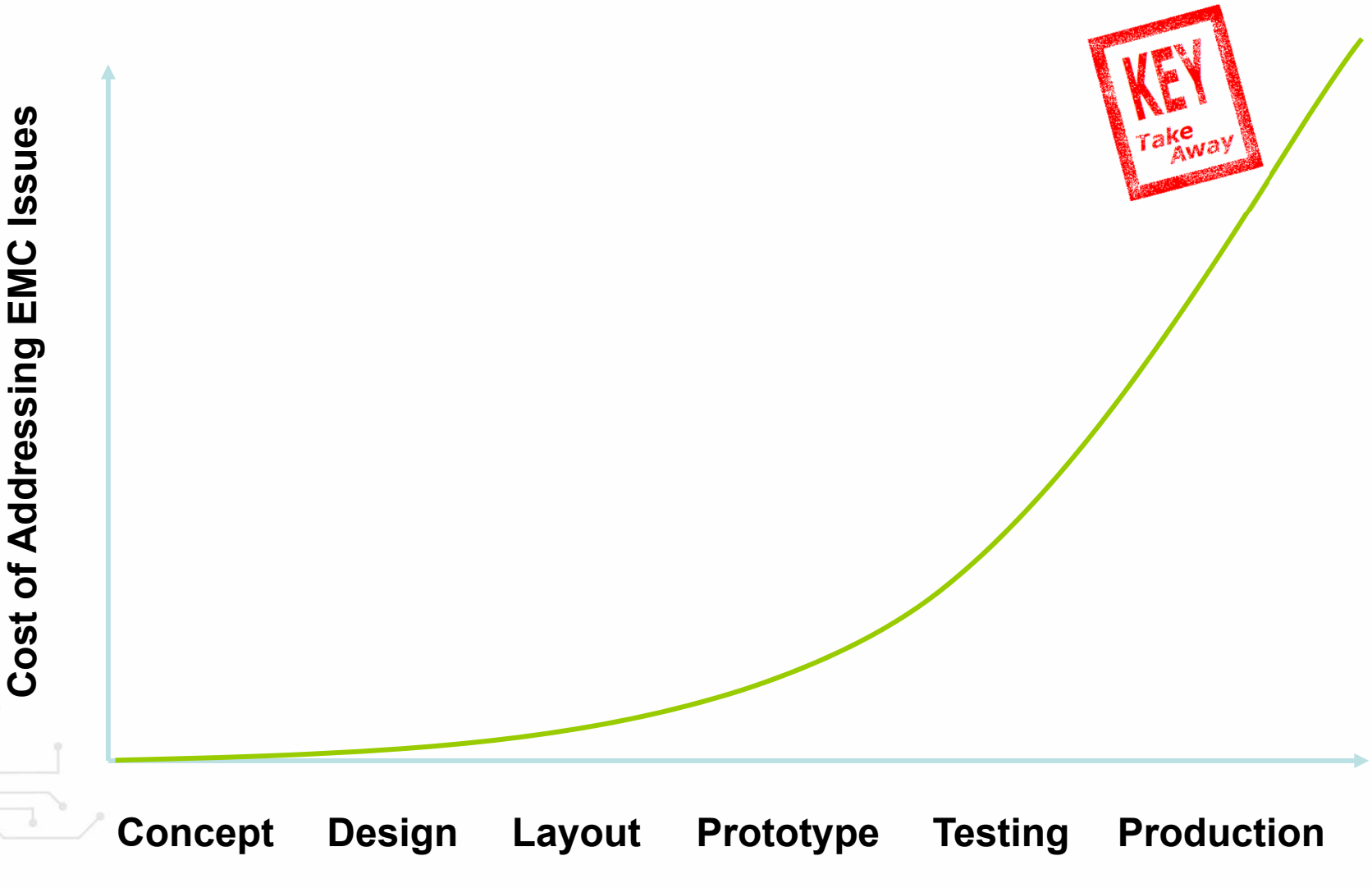
- **EMC Guideline Summary (reference)**

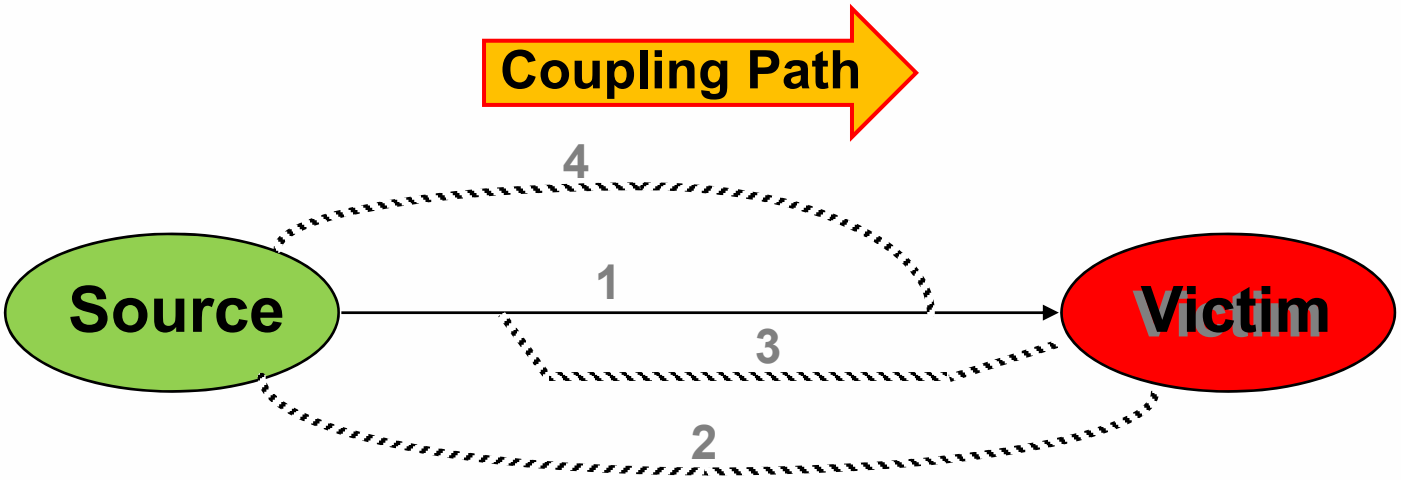
Overview of EMC

- **EMC- Electromagnetic Compatibility**
  - Capability of an electronic system to function compatibly with other electronic systems and not produce or be susceptible to interference
  - A system is electromagnetically compatible if:
    - It does not cause interference with other systems
    - It is not susceptible to emissions from other systems
    - It does not cause interference with itself

Cost of Addressing EMC



EMI Propagation Modes



1. Conducted
2. Radiated
3. Conducted/radiated (antenna effect)
4. Radiated/conducted (receiver effect)

Common EMC Standards

- **Conducted emission**
  - IEC 61000-3-2/3, EN55022: line power disturbance
  - FCC Part 15
- **Radiated emission**
  - IEC 61000-4-3
  - CISPR-11
  - FCC Part 15
- **Conducted susceptibility**
  - IEC 61000-4-4: EFT (electrical fast transients)
  - IEC 61000-4-5: lightning
- **Further information available at:**
  - http://en.wikipedia.org/wiki/List_of_EMC_directives
  - http://www.hottconsultants.com/regulations.html
  - http://www.cvel.clemson.edu/auto/auto_emc_standards.html
  - http://www.cvel.clemson.edu/emc/tutorials/commercial_emc_standards.html

ESD

- **ESD - Electrostatic Discharge**
  - **Rapid transfer of static charge between 2 objects as the result of object contact or dielectric breakdown**

ESD

Device Level

Human Body Model (HBM)
JESD22-A114B

Machine Model (MM)*
JESD22-A115A

Charged-device Model (CDM)
JESD22-C101E

System Level

IEC 61000- 4- 2

Note: Studies have shown that device level ESD is not a predictor of system level ESD

Reference: EOS/ESD Association, Inc.
https://www.esda.org/about-esd/white-papers

Note: For ESD effects on integrated circuits refer to Application Note AN1785 – ESD and EOS, Causes, Differences and Prevention

The ESD Threat

Common Static Voltages

Static Voltage as a function of Relative Humidity (RH)	20% RH kV	80% RH kV
Walking across a vinyl floor	12	0.25
Walking across a synthetic carpet	35	1.5
Picking up a polyethylene bag	20	0.6
Sliding a styrene box on carpet	18	1.5
Removing mylar tape from a PC board	12	1.5
Triggering a vaccum solder remover	8	1.0
Aerosol circuit freeze spray	15	5.0

Don’t Worry, It’s Just ESD!

Shown by kind permission of Mehdi Sadaghdar
http://www.electroboom.com

Video

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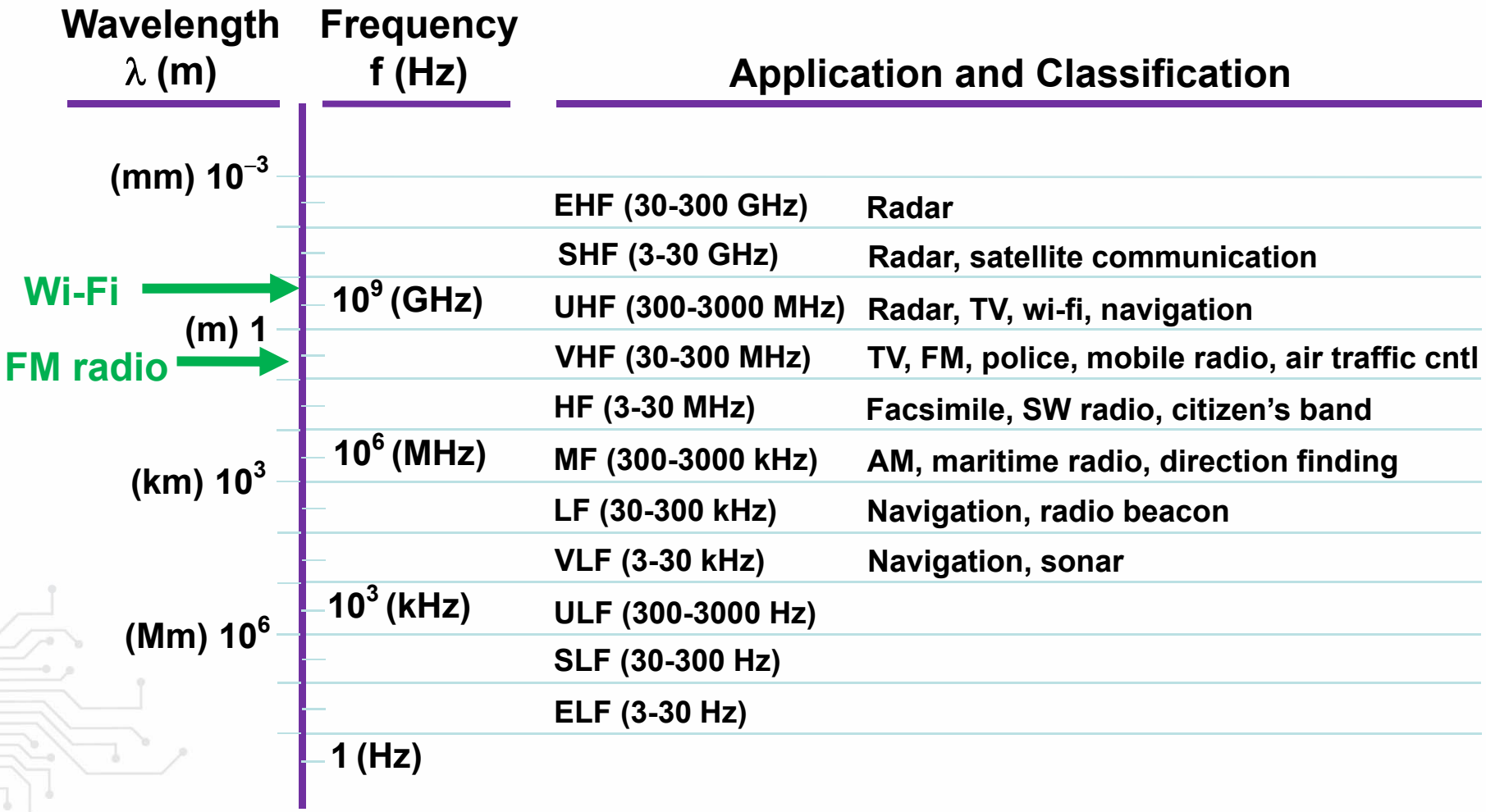
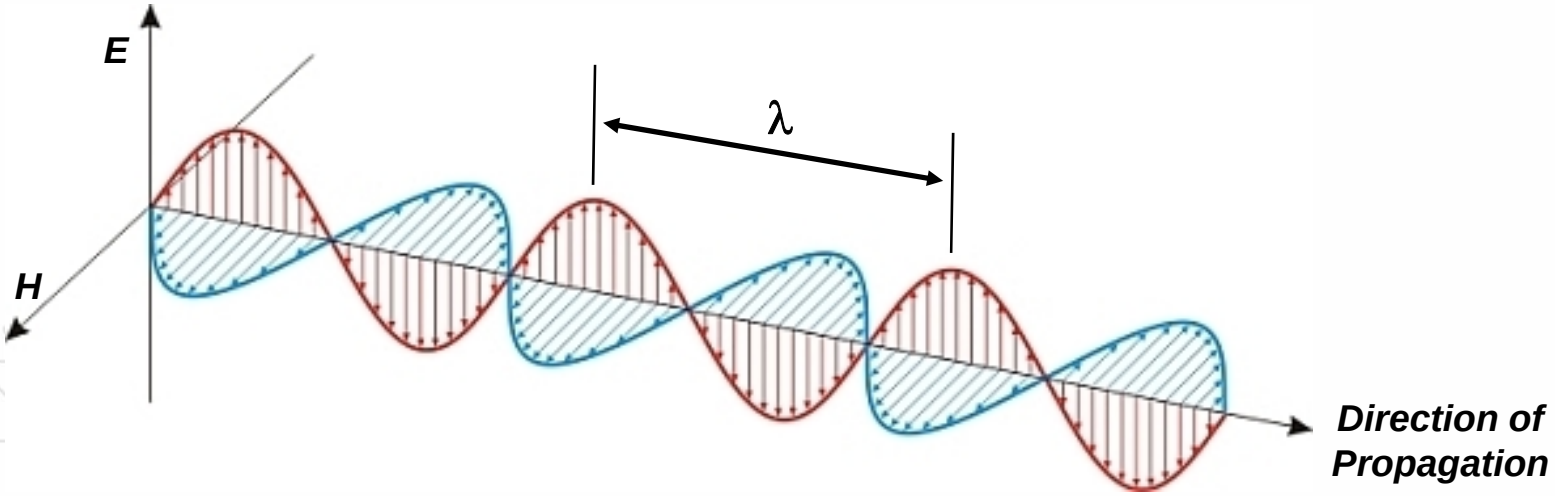
Electromagnetic Spectrum

$v = f \lambda$;where v is the speed of light in air (3×10^8 m/s)

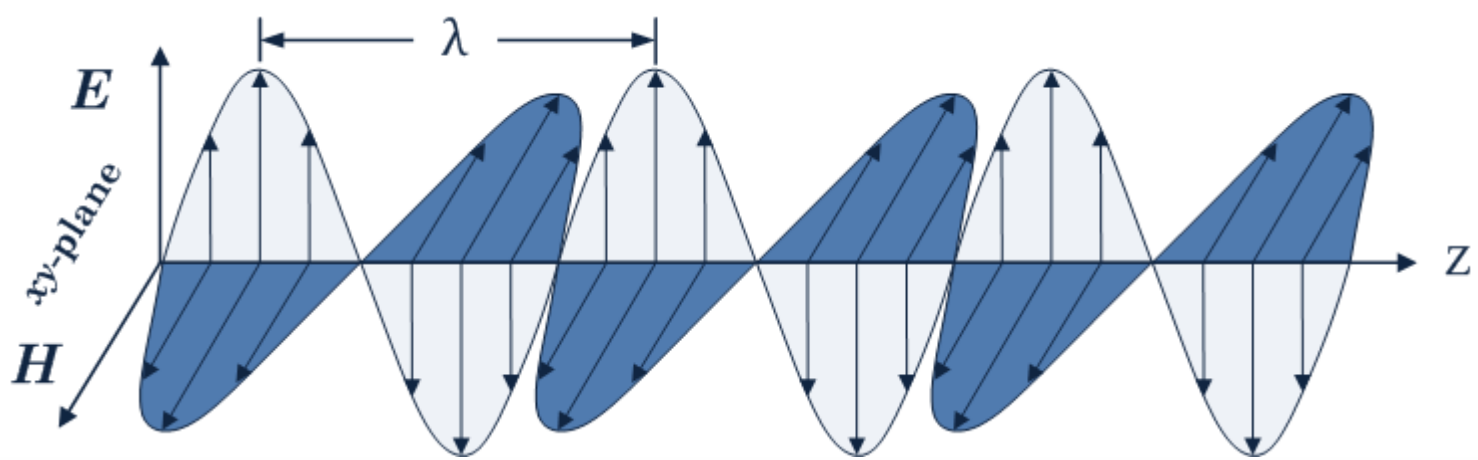


Electromagnetic wave

- **Magnetic field:**
  - Produced by charge in motion (= Current) or a magnetic dipole
- **Electric field:**
  - Produced by potential differences between points (= Voltage)



Electromagnetic wave (2)



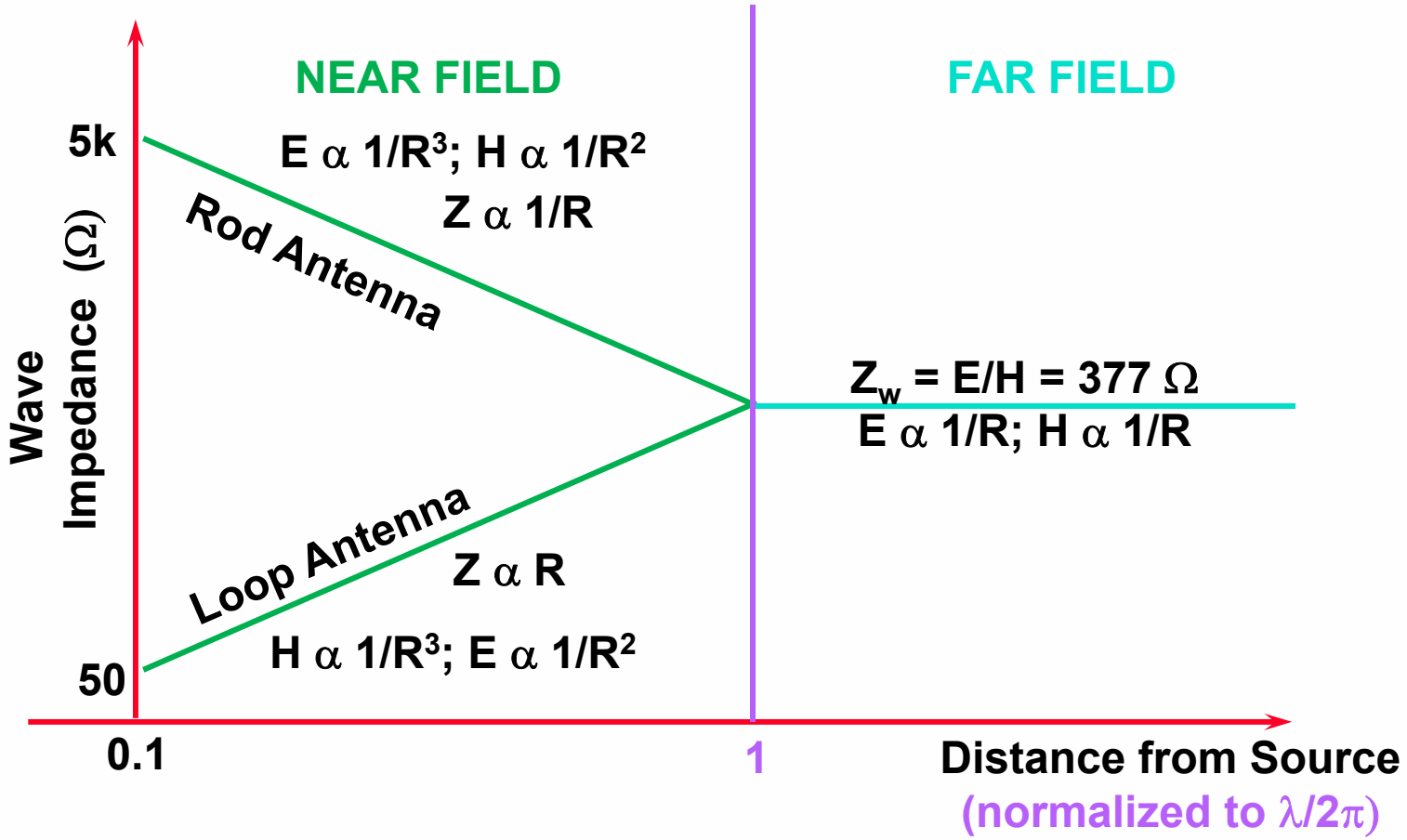
- E and H are related:

$$H = \frac{E}{Z_w}$$

For a Propagating Wave
In the Far Field

Z_w is the wave impedance of free space = 377 Ω
(often approximated to 120 π Ω)

Field Impedance



The Physics of EMC

- The field regions
  - The region with a maximum distance of $\lambda/2\pi$ is called the reactive near field
  - The region between $\lambda/2\pi$ and $2D^2/\lambda$ is the radiating near field
  - Everything in a distance of more than $2D^2/\lambda$ belongs to the far field

Near or Far Field?

- **Transition point is at $\lambda/2\pi$**
- **The higher the frequency, the closer the transition point is to the source**
- **For f_x = 2.4 GHz:**
  - λ = 12.5 cm (free space c=3x10^8 m/s)
  - Transition point = $\lambda/2\pi$ = 2 cm (approx.)
- **For f_x = 900 MHz:**

  λ = 33 cm (free space c=3x10^8 m/s)

  Transition point = $\lambda/2\pi$ = 5 cm (approx.)
- **For f_x = 100 MHz:**

  λ = 3 m (free space c=3x10^8 m/s)

  Transition point = $\lambda/2\pi$ = 47cm (approx.)

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Expressing Voltage/Current in Decibels

- Values of voltage (or current) may be expressed in dB referenced to a unity value

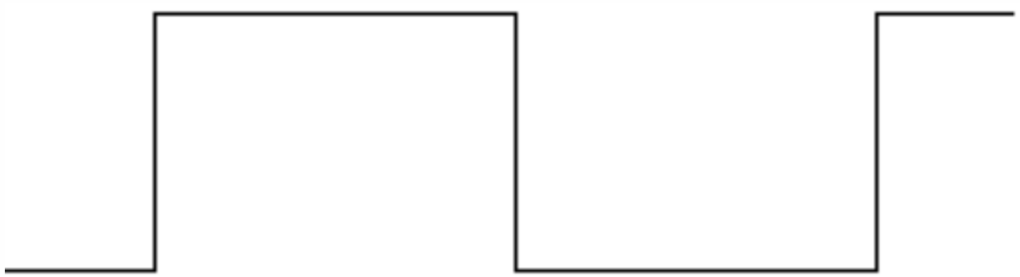
  dBV = 20log(V) -------- reference 1 V
  dBuV = 20log(uV) -------- reference 1 uV

- For example, a harmonic of 100 uV amplitude expressed in both dBV and dBuV:

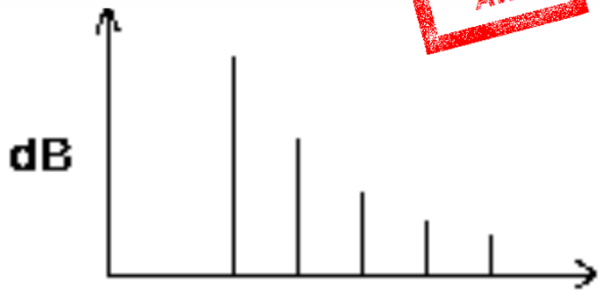
  20log(100) = 40 dBuV
  or 20log(100×10^{-6}) = -80 dBV

  Note: *n* dBV = (*n* + 120) dBuV

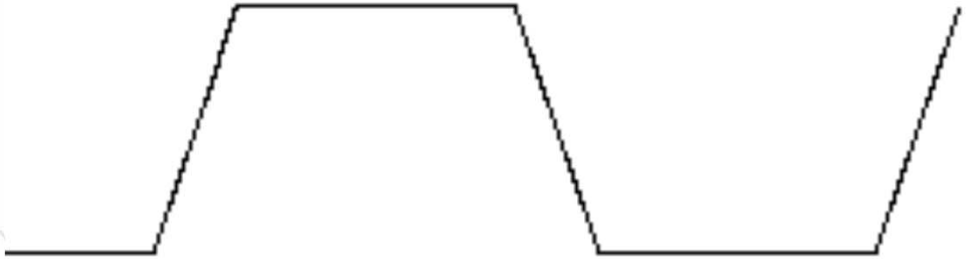
Effect of Rise/Fall Time Increase

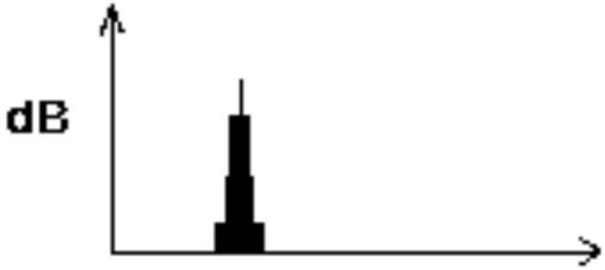


Waveform



Frequency Spectrum





The Fourier Envelope

- A graphical approximation of the peak harmonic content of a (conducted) periodic signal
- Quickly constructed for signals defined by:
  - Amplitude
  - Duty cycle
  - Period
  - Rise/fall time (use fastest edge)
- Useful to predict potential EMC problems without the need to calculate individual harmonics
- Plot key points on log-log paper

Fourier Envelope Example

where :
- A = amplitude
- t_r = rise(fall) time
- T = period
- P = pulse width

Signal Bandwidth

- **The Fourier Envelope 'knee point' is defined by:**

$$f_2 = 1/\pi t_r \ \text{Hz}$$

representing:

- The effective bandwidth of a signal above which harmonics tail off rapidly
- A reasonable upper limit for immunity, above which the device will likely not respond (this assumes that the signal represents the maximum operating frequency of the generating device)

- **This also applies to transient signals (e.g. ESD)**
  - Consequently a 1 ns ESD pulse is considered to have a 316 MHz bandwidth

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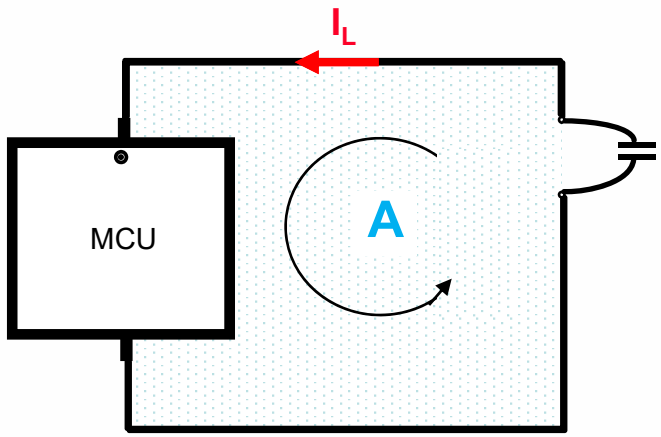
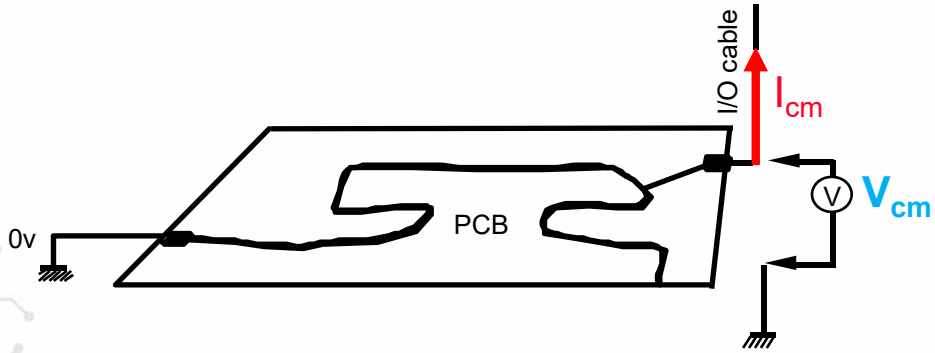
Radiation Modes



Differential mode
(loop antenna, far field)

Field strength α A I_L f^2 / distance

Due to square term, increases at 40 dB/decade

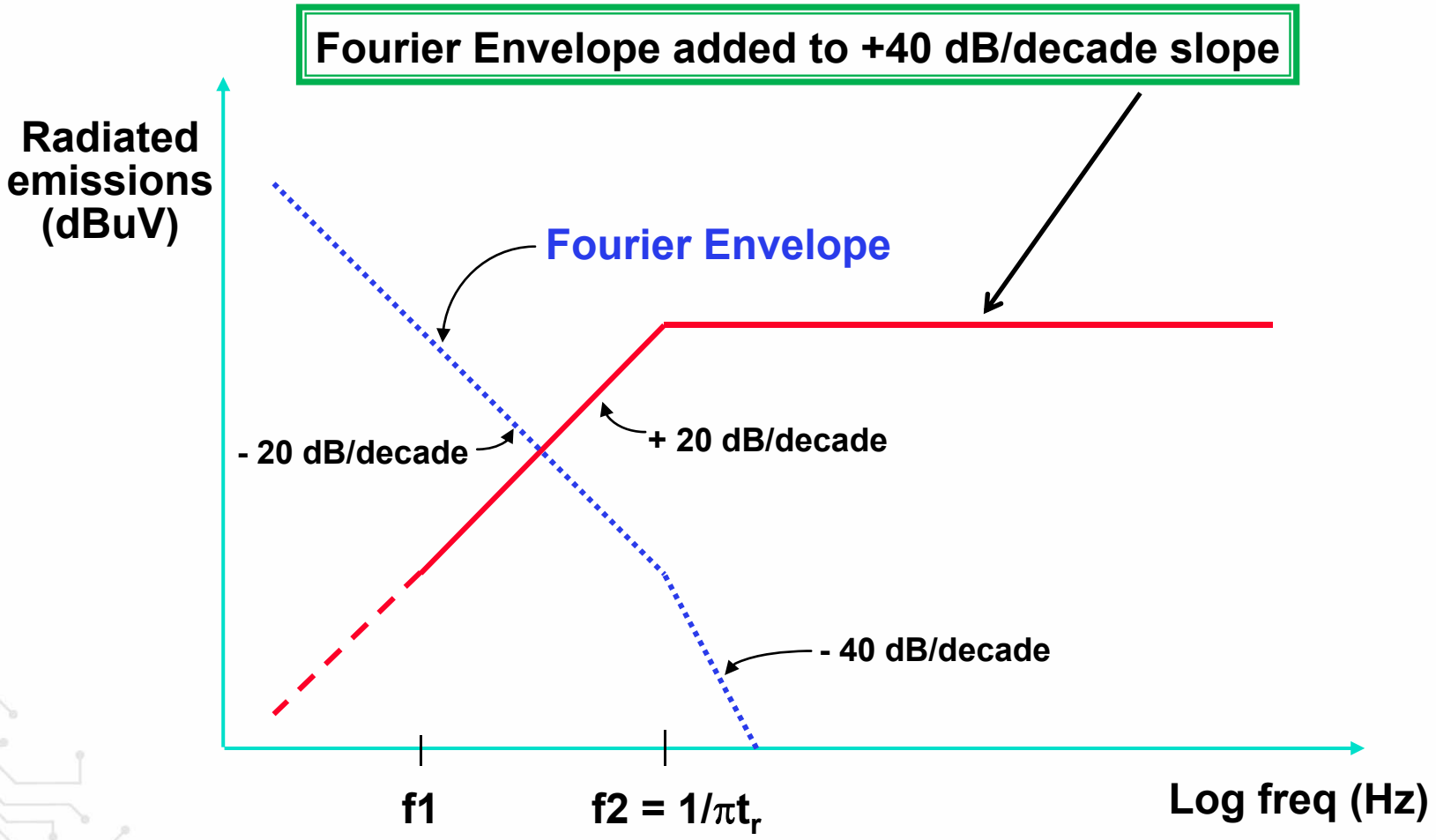


Common mode
(rod antenna, far field)

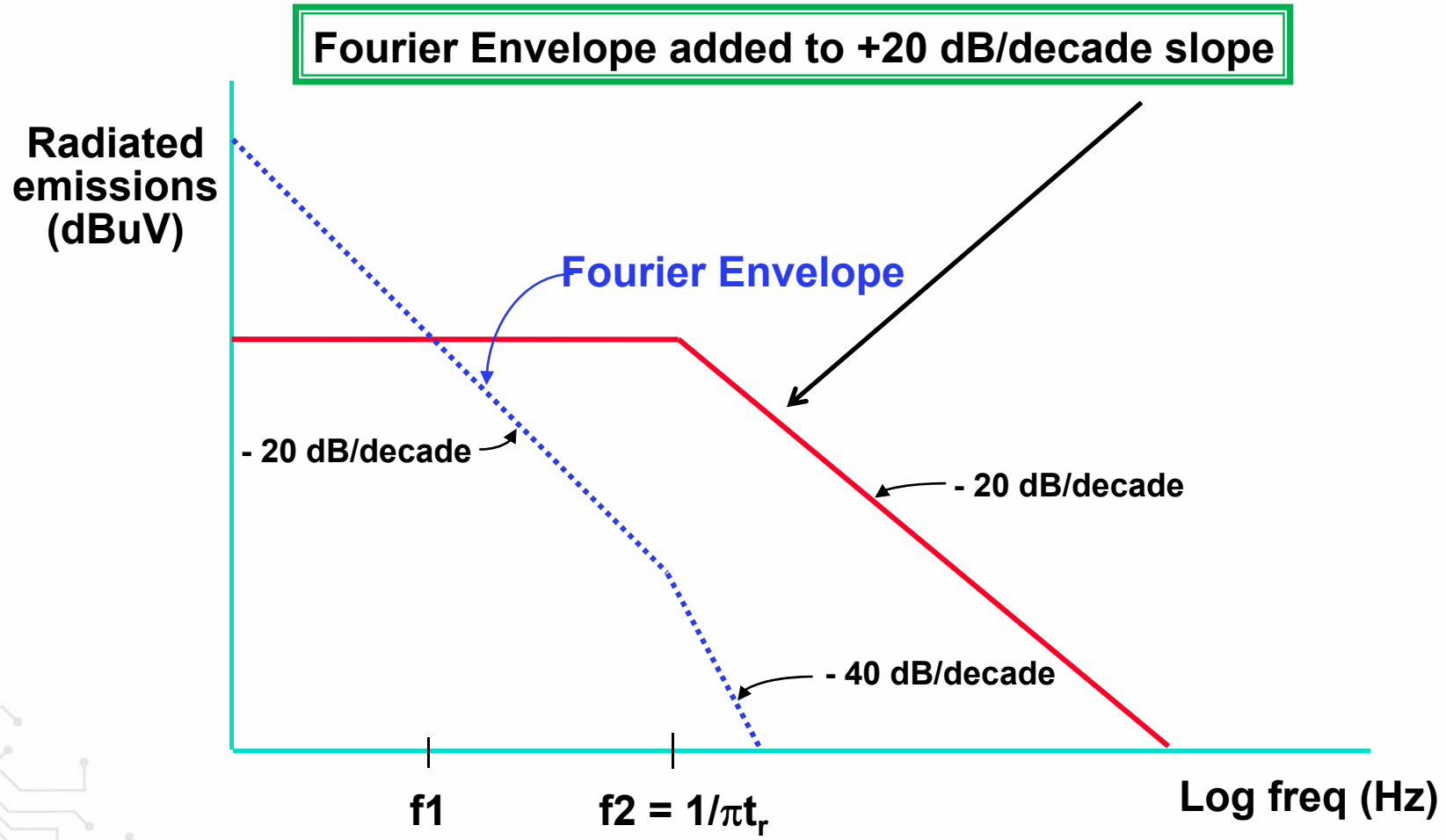
Field strength α I_{cm} f L / distance

Increases at 20 dB/decade

Radiation Efficiency: Differential Mode



Radiation Efficiency: Common Mode



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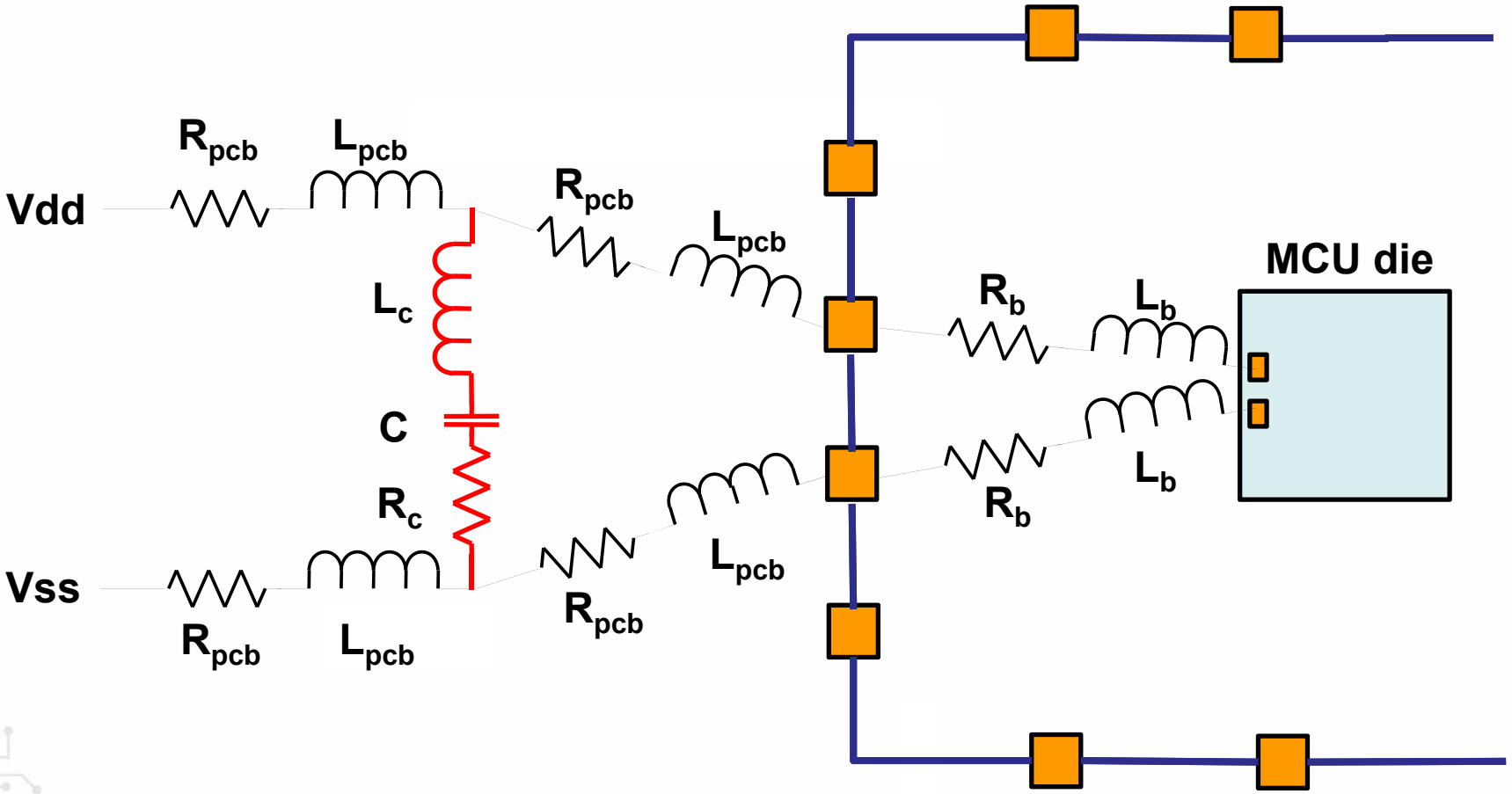
Noise Path Control

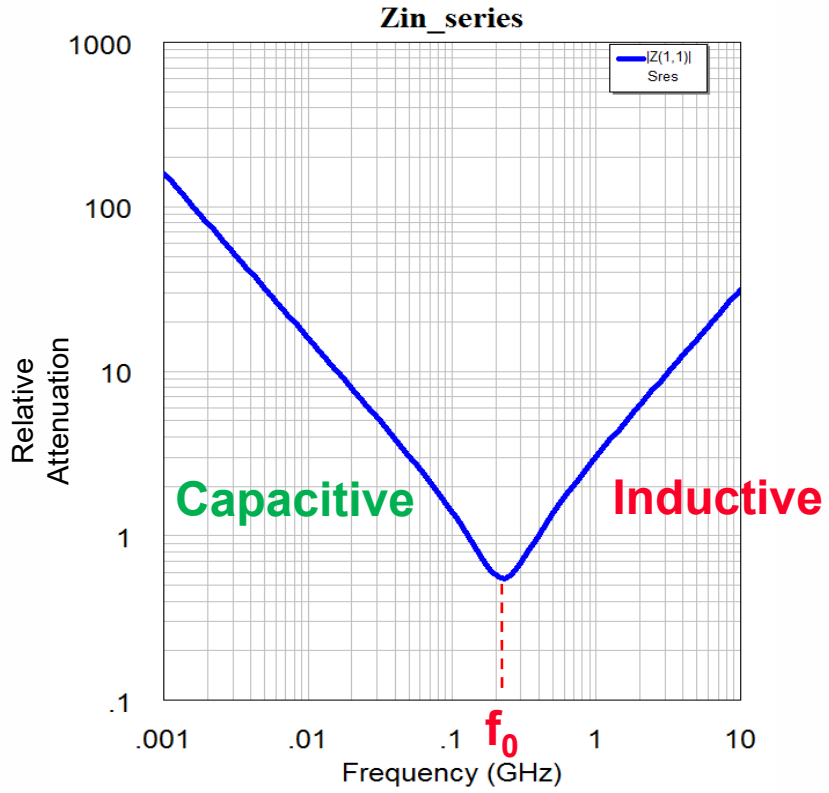
- **Decoupling**
  - Effect of imperfect passive devices
  - Parallel decoupling
  - Use of ferrite & inductors
- **Shielding**
  - How E-M shields work (or not!)
  - Effect of apertures
  - E-M field coupling
  - Shield connection guidelines

Decoupling of a Vdd Pin

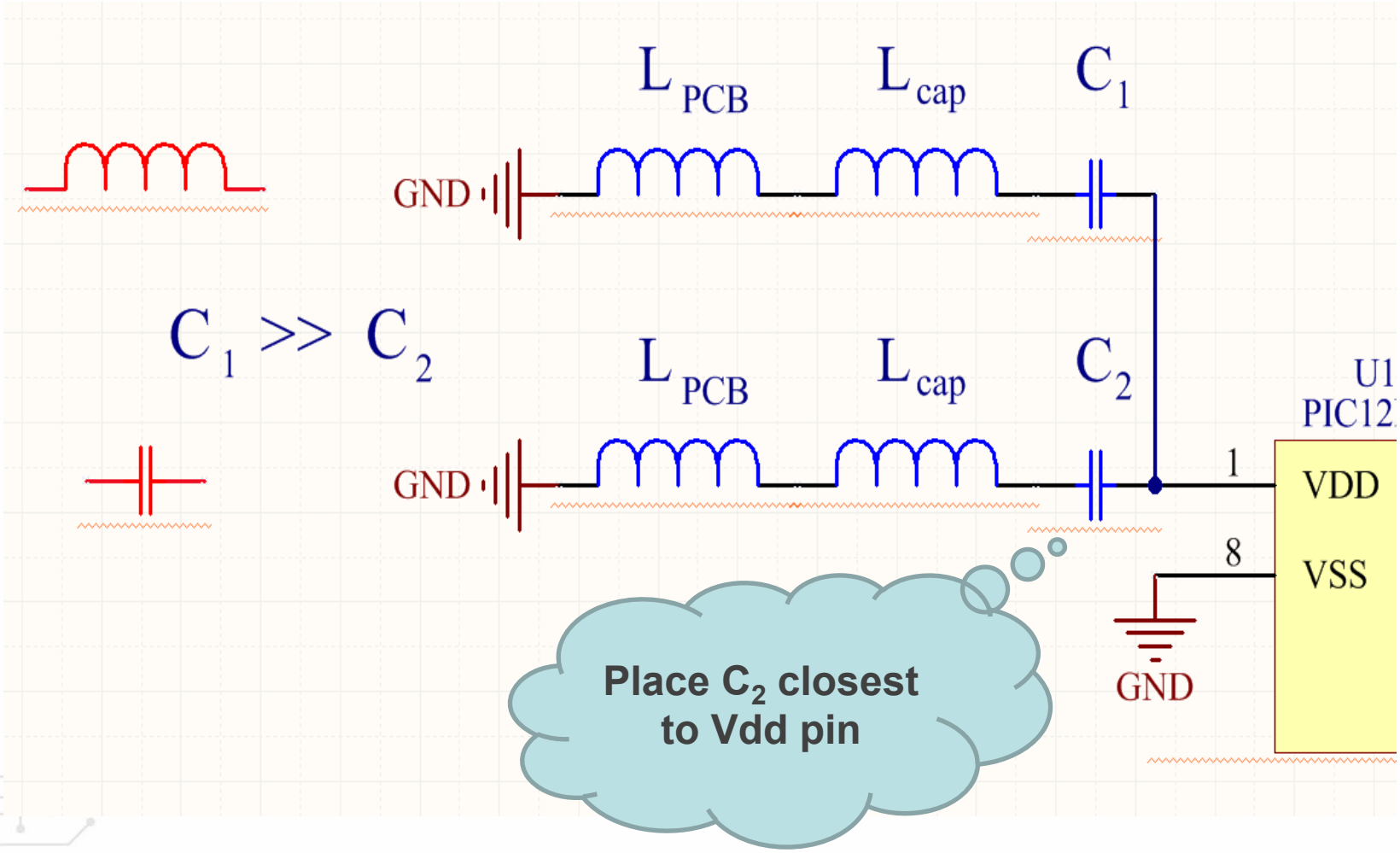


Series Resonance

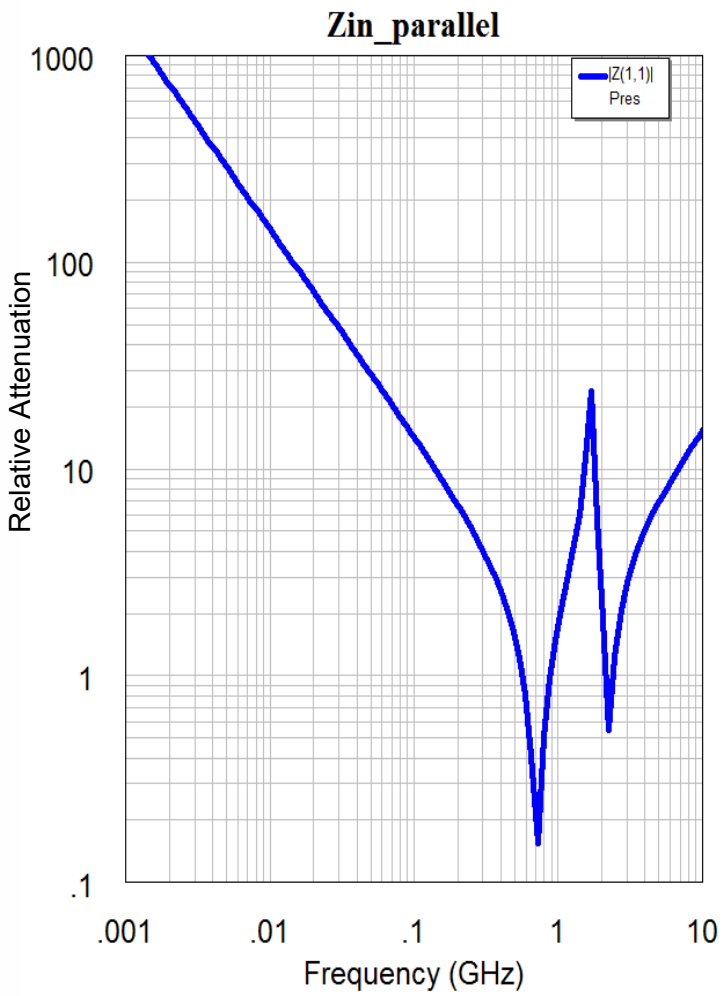
- At frequencies above f_0, the capacitor becomes inductive (and ineffective)



Unwanted Parallel Resonance

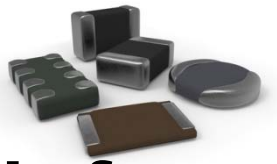


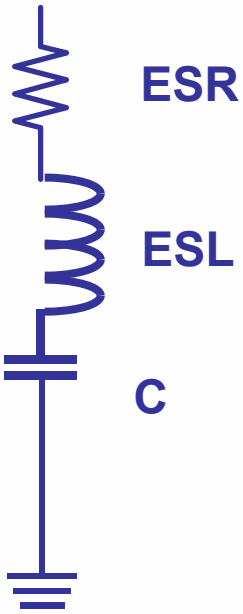
Series and Parallel Resonance



Bypass Capacitor Types

- **Filters Noise at High Frequency:**
  - Ceramic – Small case size, inexpensive,
  - Fair stability, low inductance
    - X7R / X5R – cost effective





- **Acts as a Charge Reservoir for Slower Current Demand**
  - Tantalum Electrolytic – Small size, large values, medium inductance

  - Hi-K ceramic – Small size, medium values, low inductance, voltage dependent
  - Aluminum Electrolytic less preferable due to high self inductance

Choosing a Capacitor Type

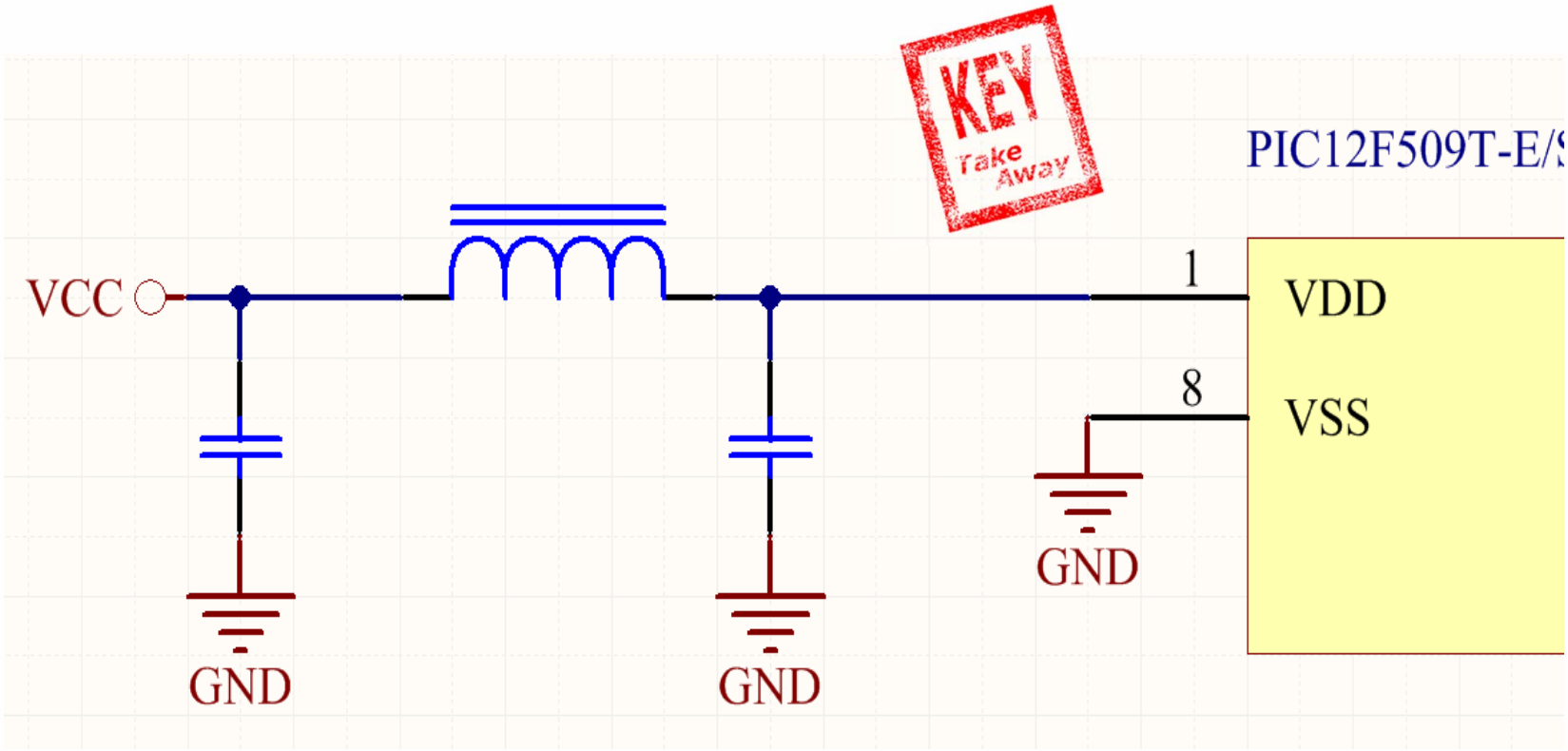
Type	Max Useable Freq
Aluminum electrolytic	1 -> 250 kHz
Tantalum electrolytic	1 kHz -> 1 MHz
Hi-K ceramic (surface mount)	100 kHz -> 100 MHz
Polyester film (leaded)	1 -> 100 MHz
Low-loss ceramic	1 -> 10 GHz

- Choose a capacitor type to cope with the highest expected in-band harmonics
- Remember, lead and trace inductance can lower self-resonance point and significantly reduce overall frequency response!

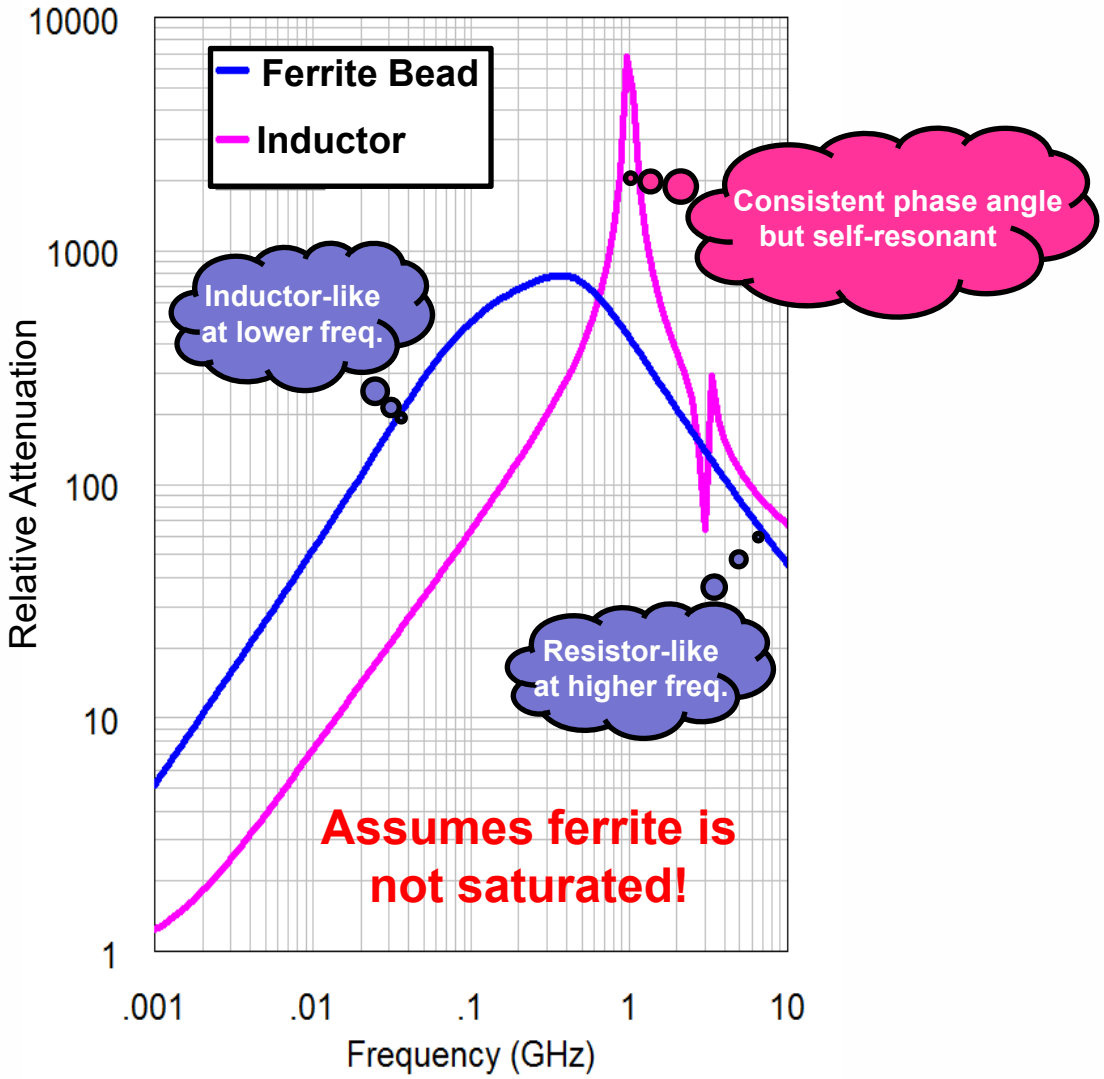
Ceramic Capacitors: Beware Voltage Effects

- **Class 2/3 ceramic caps can have significant applied voltage bias coefficients in addition to temperature coefficients**
  - Actual capacitance can be 50% lower than rated (nominal) value at higher bias!
    - Dissipation factor (inverse of Q) also increases with applied voltage
  - Higher the volumetric efficiency (dielectric K), the more pronounced the effect
    - Select caps with operating temperature, frequency *and* voltage ranges in mind (not just cost)

Decoupling Power with Low Pass Filter



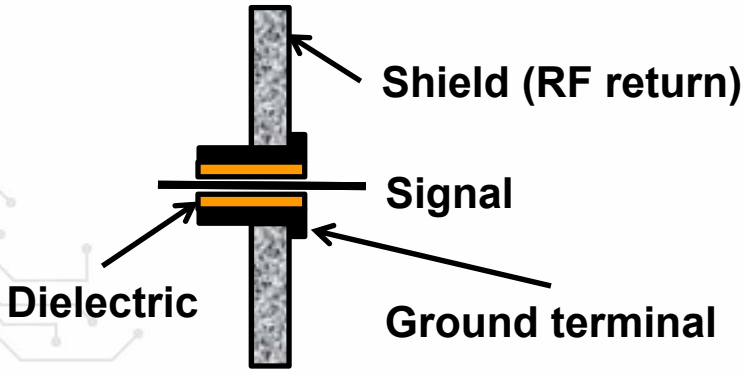
Inductor vs. Ferrite Bead



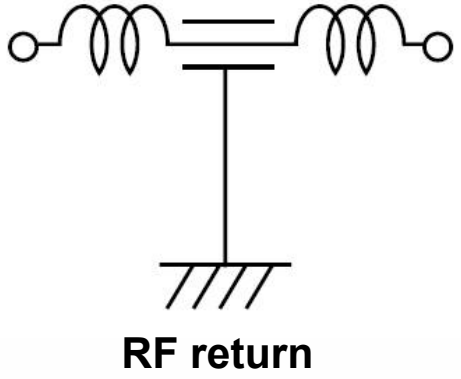
Decoupling Signals with A Feedthrough Capacitor

- **Feedthrough capacitors create an efficient low-pass filter for signals**
  - Effectively zero RF return inductance
  - Improved insertion loss characteristics (compared to a leaded cap of same value)
  - Commonly found in low-EMI system/PCB connectors

Feedthrough Capacitor Example



Equivalent Circuit



Noise Path Control

- Decoupling
  - Effect of imperfect passive devices
  - Parallel decoupling
  - Use of ferrite & inductors
- **Shielding**
  - How E-M shields work (or not!)
  - Effect of apertures
  - E-M field coupling
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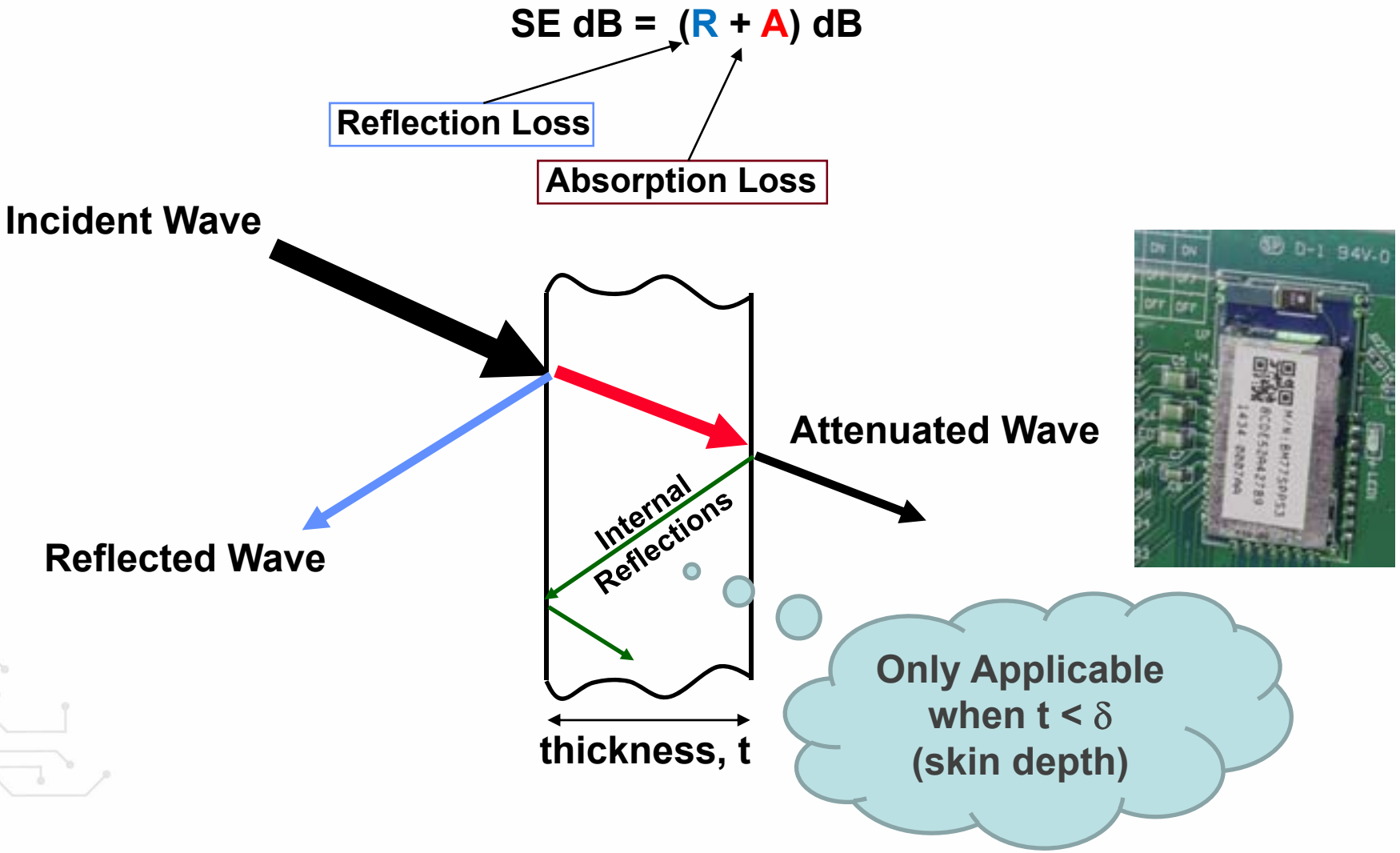
Shielding Effectiveness (SE)



Absorption loss

$$A/_{dB} = 20 \cdot lg \; e^{\frac{t}{\delta}}$$

t = shield thickness
δ= skin depth

The skin depth is:

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}}$$

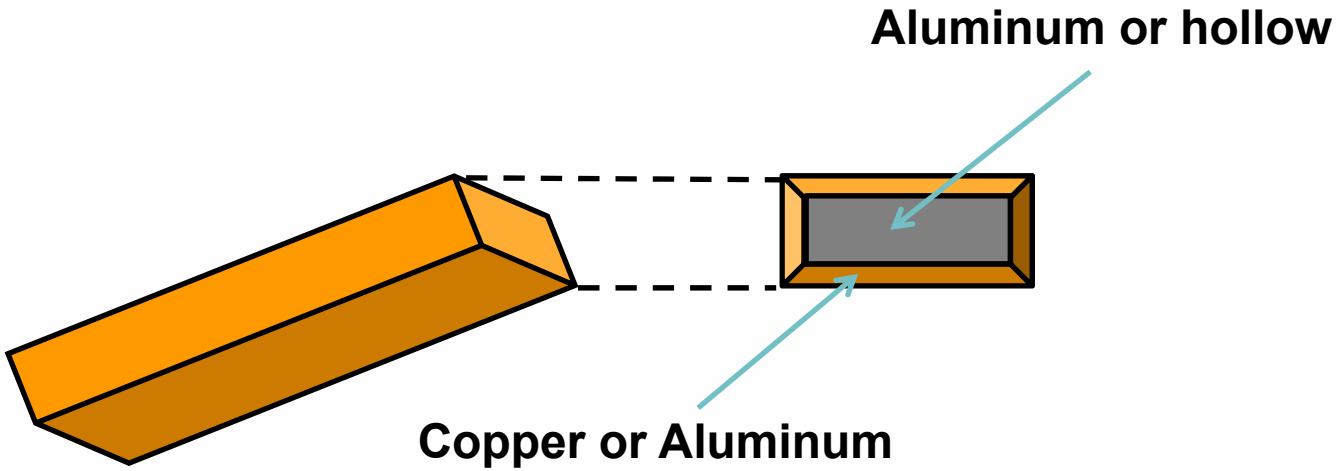
f = frequency in Hz
μ = permeability in H/m
σ = conductivity in S/m

For example copper:

Frequency f	Skin depth δ	Absorption loss for 35μm shield
50 Hz	9.3 mm	0.03 dB
10 kHz	0.66 mm	0.46 dB
100 kHz	0.21 mm	1.45 dB
1 MHz	66 μm	4.6 dB
10 MHz	21 μm	14.5 dB
100 MHz	6.6 μm	46.1 dB

Practical Skin Depth Example

- **High current power bus bars**
  - Only the first few cm are made from copper or aluminum



Reflection loss: Radiator in the far field

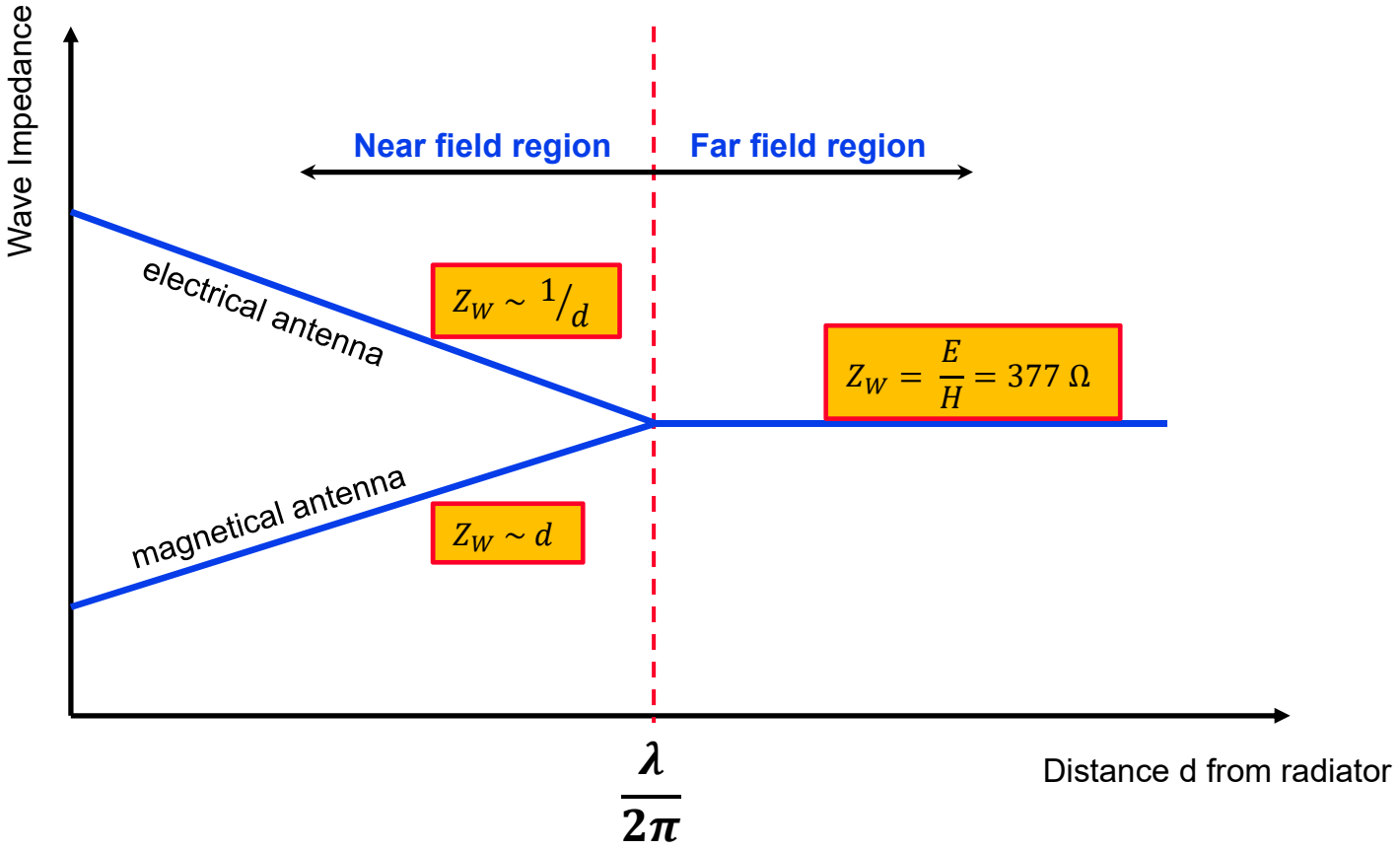
Plane wave at normal incidence to a plane shield:

$$R/_{dB} = 168 + 10 \cdot lg \frac{\sigma_r}{\mu_r \cdot f/_{Hz}} \qquad \left(\sigma_r = \frac{\sigma}{\sigma_{copper}}\right)$$

Reflection loss is:

- independent on shield thickness
- decreasing with increasing frequencies
- larger for high conductivity materials

Shielding: The field impedance



Reflection loss: Radiator in the near field

$$R/_{dB} = 20 \cdot lg \frac{Z_W}{4 \cdot Z_S}$$

with:

$$Z_S = 3.68 \cdot 10^{-7} \cdot \sqrt{\frac{\sigma_r \cdot f/_{Hz}}{\mu_r}} \ \Omega$$

- large Z_W and low Z_S gives good shielding (electrical radiator)
- magnetical radiator is poorly shielded by copper
- for magnetical radiator use high μ_r

Shielding Summary

- **E-fields and (far field) plane waves are relatively easy to successfully shield with thin, high conductivity material**
  http://www.cvel.clemson.edu/emc/calculators/SE_Calculator/index.html

- **Near field H-fields are more difficult to shield especially at low frequencies. Use high permeability material**
  http://www.cvel.clemson.edu/emc/calculators/SE_Calculator/nearfieldSE.html

- **Practical shields are invariably imperfect so actual shielding effectiveness values attained are always less than those theoretically derived!**

Shield Failures

- **There are two primary causes of shields not coming close to the predicted shielding efficiency:**
  - Leakage at slots (gaps, seams)
    For E-M waves, the area of a hole in a shield is of less importance than its length. Slots act as antennas - even thin slots can leak a lot of energy if they are long enough
  - Penetration of the shield with a conductor
    Any conductor passing through a shield to which it is not terminated will provide free passage for RF energy past the shield. The “hole” dimension makes little difference

Apertures: Slot Antenna

- **Leakage is proportional to L and f (frequency) such that:**

SE = 20log(λ/2L) dB
= 20 dB for L = λ/20 (15 cm @100 MHz)
= 40 dB for L = λ/200 (1.5 cm @100 MHz)

- **Keeping slot length less than λ/20 of the highest frequency you want to shield will provide >20 dB SE**
  - Accounts only for effect on reflection SE
  - Real shields will likely be several skin depths thick, so will also contribute absorption loss

Multiple Apertures: Slots

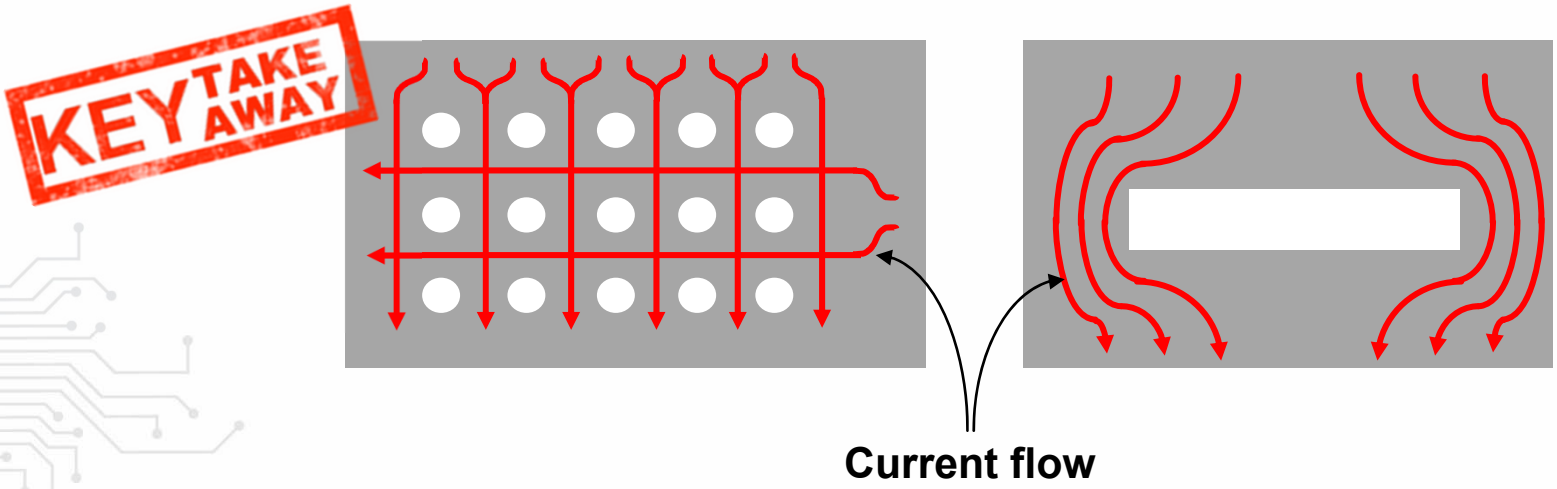
- **Multiple similar, linearly spaced apertures will reduce SE roughly by the square root of the number of apertures, n**

$$SE_{(lost)} = 20\log(n)^{1/2}\ dB$$

- **But does not apply to same number of apertures placed on different enclosure surfaces!**
  - Radiation is not all in the same direction

Multiple Apertures: Holes

- **Small holes perturb the shield current much less than slots do because only the first discontinuity (first row/column) really affects SE**
  - First row/column approximately equivalent to one set of multiple, linearly spaced, apertures
  - Current flow relatively unperturbed thereafter
- **An array of holes will therefore leak less than a single slot of an equivalent total area (e.g., microwave oven)**



Apertures: Circular Waveguides

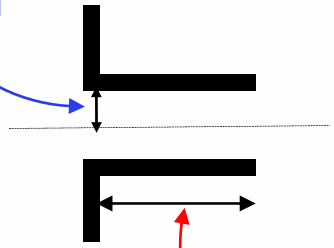
- Extending the shield wall into a hole makes it into a waveguide the attenuating effect of which (when operated below its cutoff frequency[1]) is approximated as:

$$SE \cong \frac{16T}{R} \quad dB$$

where: T = depth (cm)
R = diameter (cm)
(and T > R)

Radius = 0.25 cm

$$SE = \frac{16 \times 2}{0.25} = 128 \text{ dB}$$



Depth = 2 cm

Note 1:

$f_c = 1.841c / 2\pi R$
$\cong 8.8 \times 10^9 / R$
$\cong 35$ GHz

By way of comparison, best screen room will attenuate by 120dB!

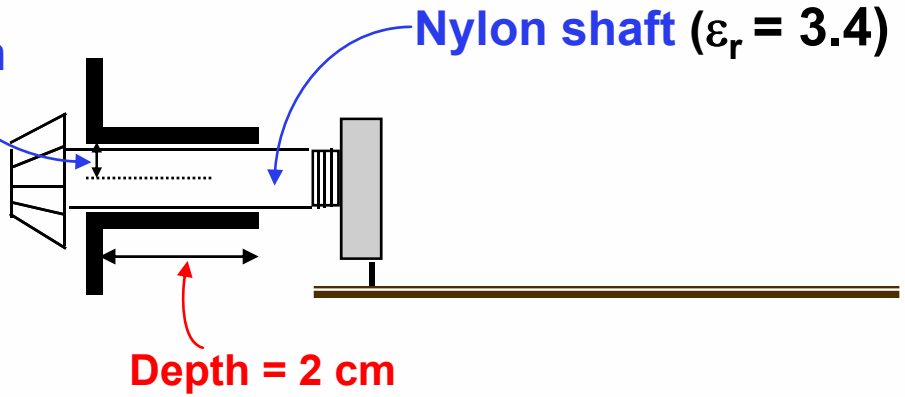
Apertures: Circular Waveguides

- Adding a dielectric material into a waveguide reduces *c* and consequently SE:

$$SE \cong \frac{16T}{R(\varepsilon_r)^{1/2}} \text{ dB}$$

where: T = depth (cm)
R = radius (cm)
(and T > R)
ε_r = relative dielectric constant

$$SE = \frac{16 \times 2}{0.25 \times (3.4)^{1/2}} = 69 \text{ dB}$$



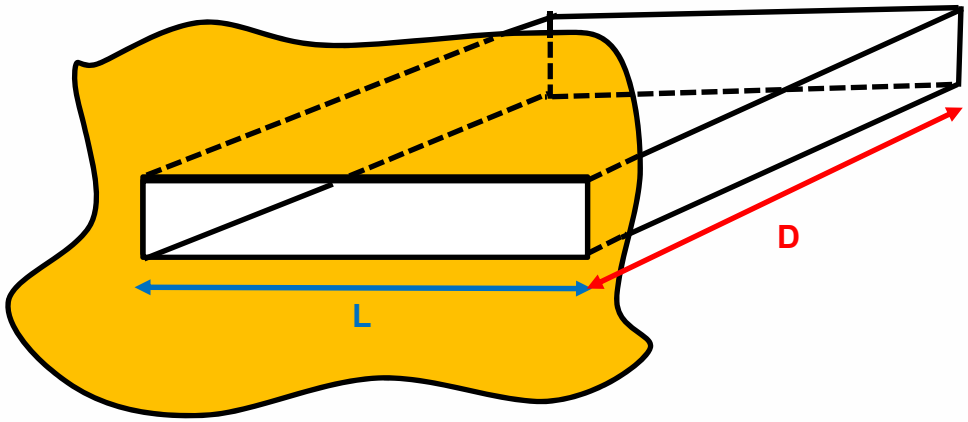
Apertures: Rectangular Waveguides

- A rectangular hole can also become a waveguide by extending it through a shield, the attenuating effect of which (when operated below its cutoff frequency[1]) is approximated as:

$$SE \cong \frac{27D}{L} \text{ dB}$$

where: D = depth (cm)
L = length (cm) and height << L
(and D > L)

$$SE = \frac{27 \times 4}{2} = 54 \text{ dB}$$

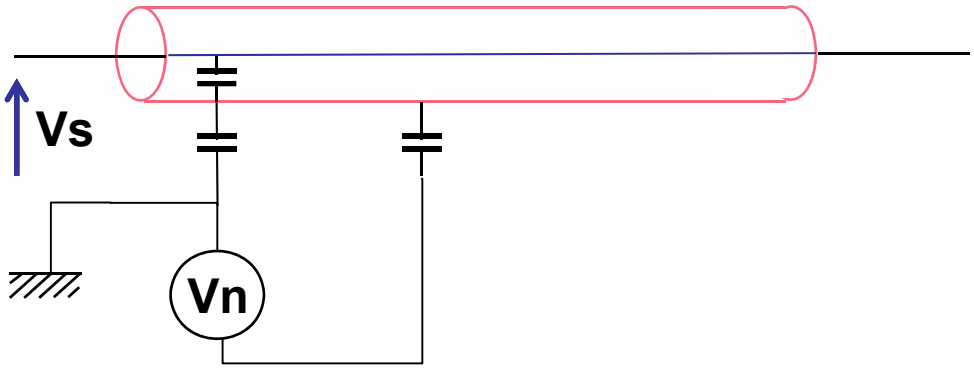


Note 1:

$f_c = 100c / 2L$
$\cong 1.5 \times 10^{10}/L$
$\cong 7.5$ GHz

Shielded Cable: Electric Field Coupling

- **Can be modeled with capacitances. Assuming a perfect shield:**
  - If shield not grounded, Vs = Vn
  - If shield grounded, Vs = 0
- **Conductor length beyond shield unprotected so must be minimized**
- **Shield ground must have minimum inductance and remain effective throughout shield length**

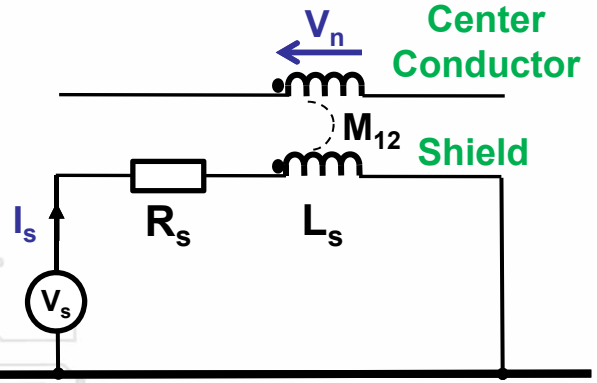


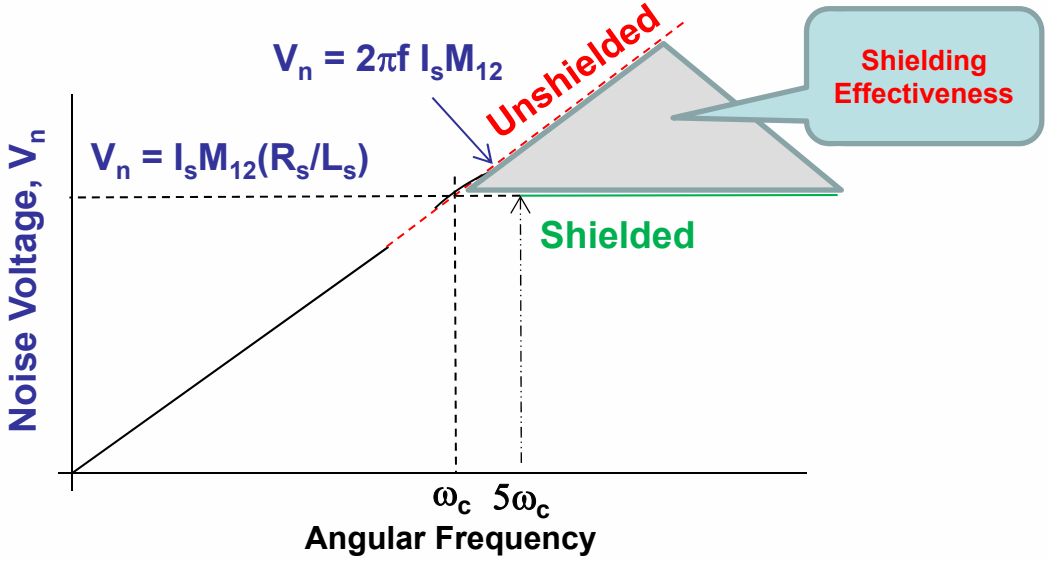
Shielded Cable: Magnetic Field Coupling

- Can be modeled with inductances
- Shielding Effectiveness limited by mutual inductance between shield and center conductor
  - Cut-off frequency below which SE minimal is: $\omega_c = R_s/L_s$

Note: Rs/Ls includes entire current return path Z. Minimize to reduce ω_c (i.e., do not terminate shield with a resistor!)

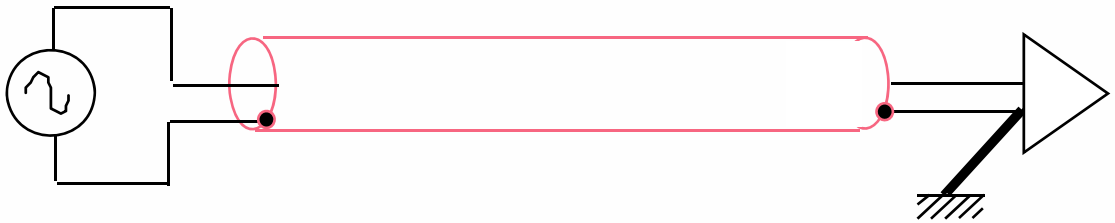
  - At f > 5 ω_c , shield and center conductor noise currents (and resultant fields) cancel
  - At f < 5 ω_c , shield Z effectively increases, and more current starts to return via return plane





Shielded Cable: Grounding for Low Frequency

- **For digital f < 5kHz or any audio signal, ground at one end only to eliminate ground loops**
  - At low frequencies, grounding at both ends can result in common mode (source + induced noise) return loop currents to flow through shield
    - Low f skin depth >> shield thickness, so common mode currents flow on both sides of the shield and therefore add to source return current at the amplifier
    - At frequencies < ω_c , magnetic shielding poor anyway (i.e., shield Z rises



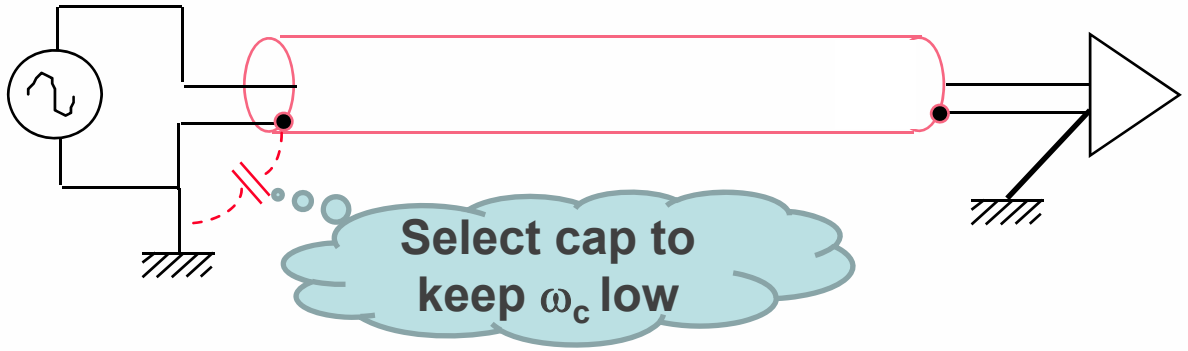
Grounded amp, ungrounded source

Ungrounded amp, grounded source

Shielded Cable: Grounding for High Frequency

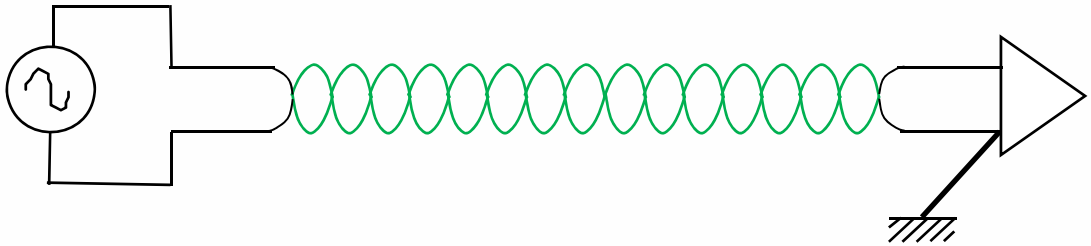
- **Ground shield at both ends when:**
  - Shielding a digital signal where f > 5kHz

  or
  - The shield length exceeds $\lambda/20$ of the highest frequency of interest (electrically long cables)
- **Keep lead lengths short; never use pigtails for high frequencies!**
- **Always ensure that shield grounds are noise free**
- **Use a high frequency capacitor to provide a DC block at low frequencies and break the LF 'ground loop'**



Using Twisted Pair

- **Low frequency common mode current effects can be mitigated using unshielded twisted pair (UTP)**
  - UTP should only be grounded at one end only to avoid ground loops



Grounded amp, ungrounded source

- **Shield twisted pair (STP):**
  - At low frequencies, separates source and shield (noise) return paths
  - At high frequencies, provides benefits of both UTP and coax
  - Ground based on frequency of interest

Agenda

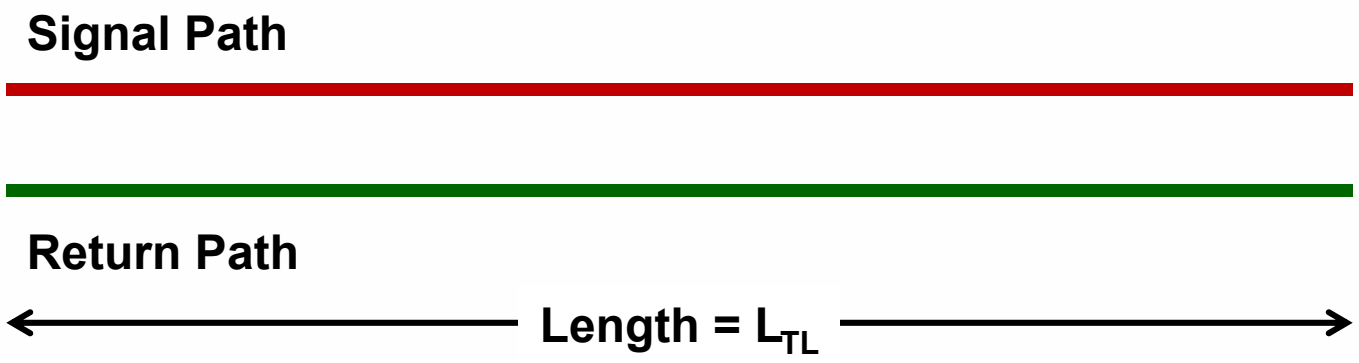
- What is ‘EMC’ and Why We Care About It
- Characteristics, Quantification and Radiation Modes of Electrical Noise
- Noise Path Control
- **Signal Integrity**
- Design for EMC
  - Circuit Design for EMC
  - PCB Design for EMC
- Real-Life EMC ‘uh-ohs’!
- EMC Guideline Summary (reference)

Signal Integrity

- Transmission Lines
- Termination Schemes
- Methods of Crosstalk
- Mitigating Crosstalk

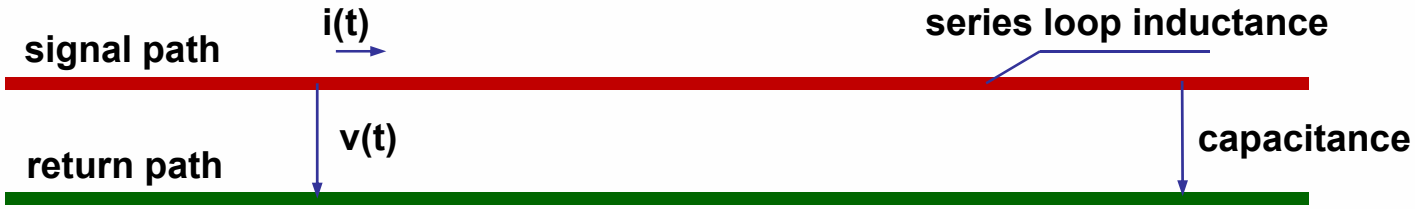
What are Transmission Lines?

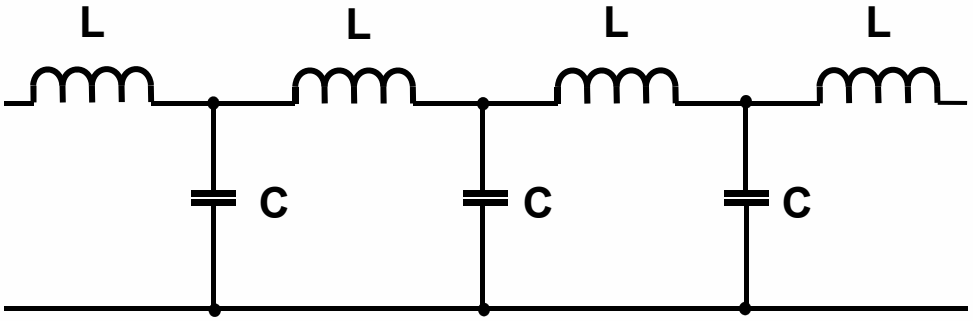
- Two conductors that have some quantifiable length.



- Return Path commonly referred to as ground. Technically correct, but can also be a power plane.

Lossless Transmission Line Characteristic Impedance



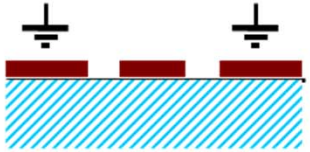


$$Z_0 = \sqrt{\frac{L}{C}}$$

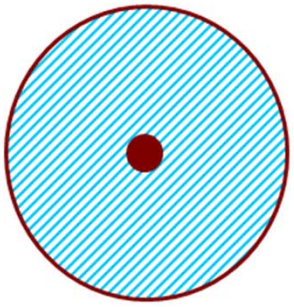
Transmission line examples

Twin lead

Microstrip

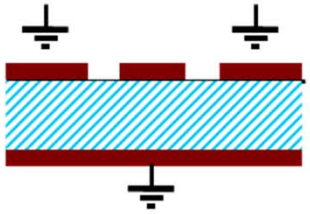


Coplanar



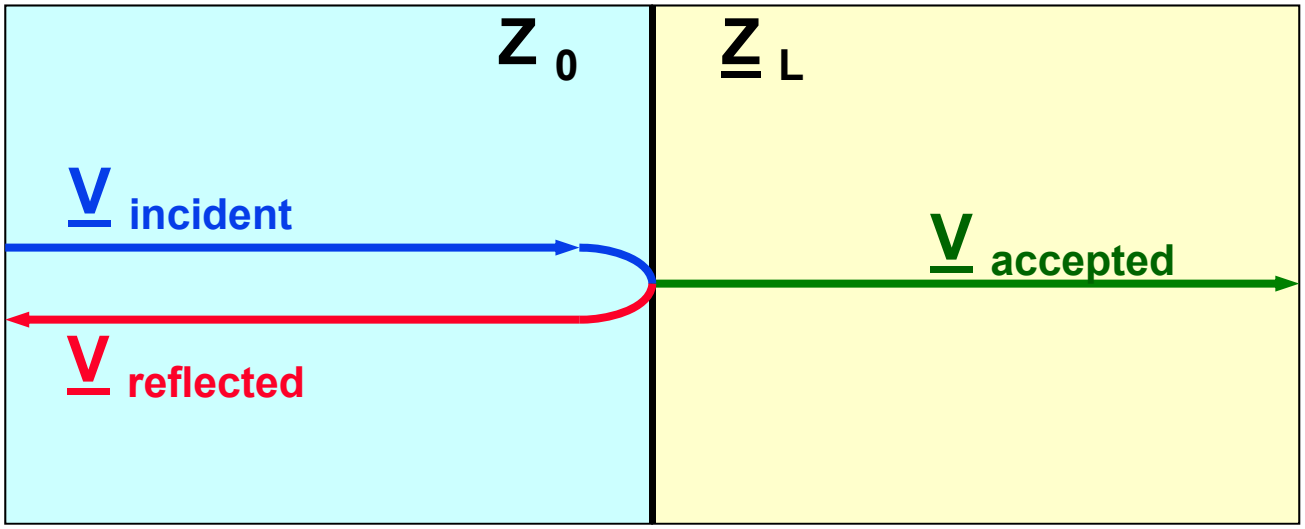
Coaxial

Stripline



Grounded coplanar

Reflection at discontinuities

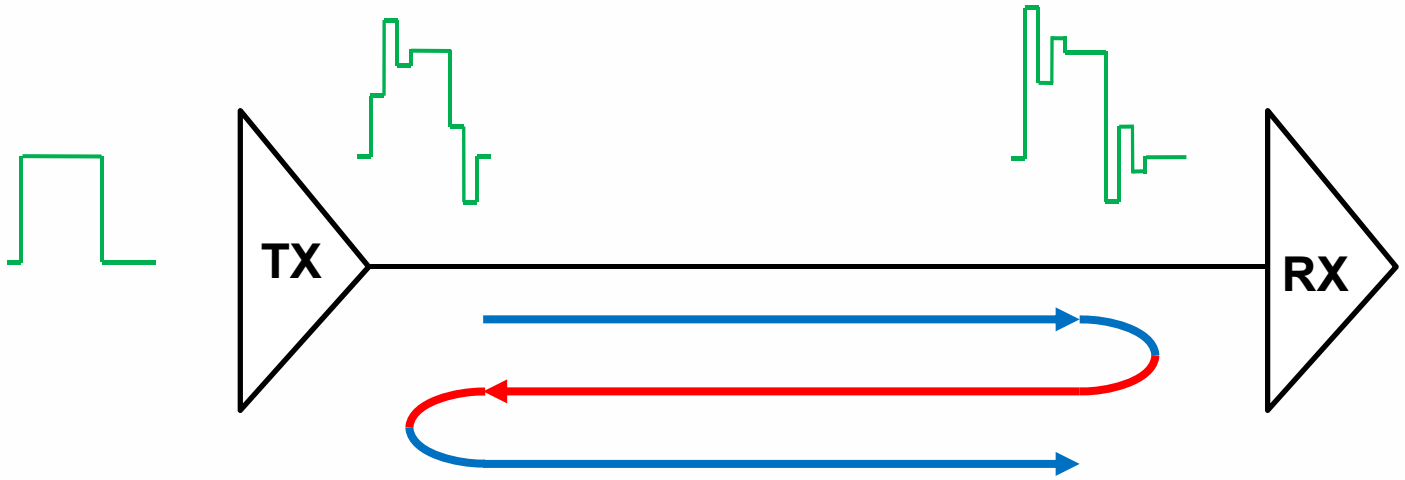


$$\underline{\Gamma} = \frac{\underline{V}_{reflected}}{\underline{V}_{incident}} = \frac{\underline{Z}_L - Z_0}{\underline{Z}_L + Z_0}$$

$$\underline{\Gamma} = \left|\underline{\Gamma}\right| \cdot e^{j\varphi_\Gamma}, \left|\underline{\Gamma}\right| = \rho$$

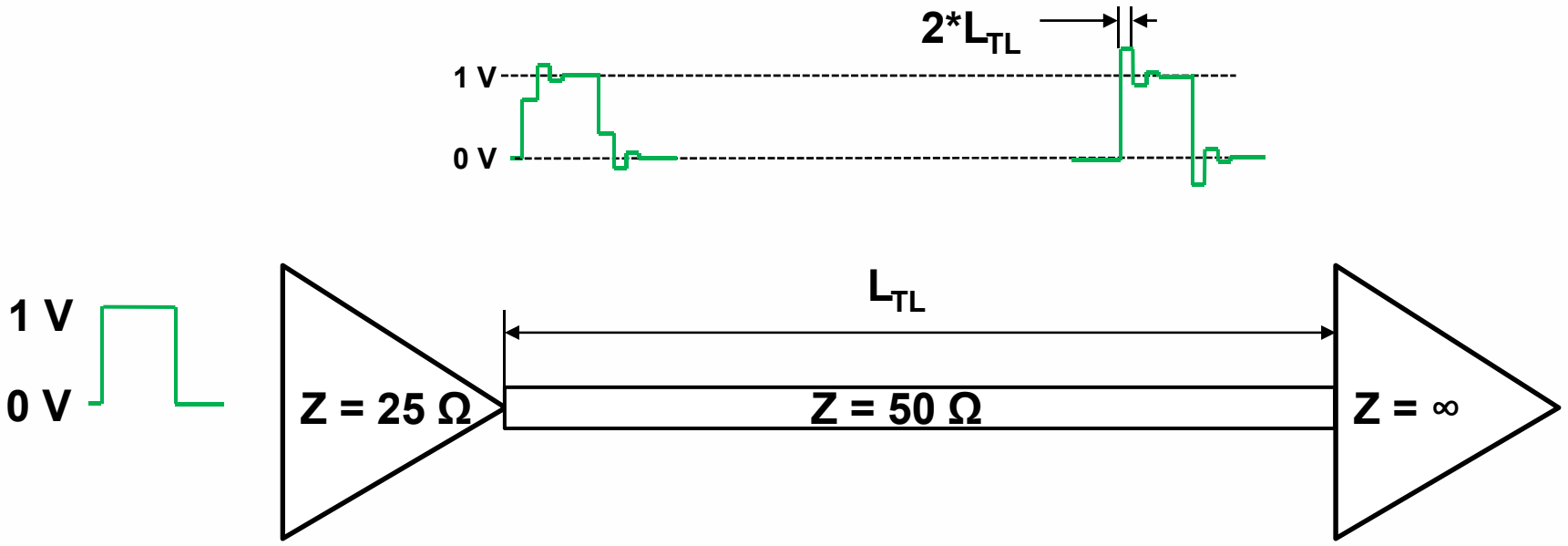
KEY Take Away

Multiple Reflections



- Propagation time (t_{prop}) dependent on transmission line and material types:
  - Microstrip in FR4: ~160 ps/in
  - Stripline in FR4: ~180 ps/in

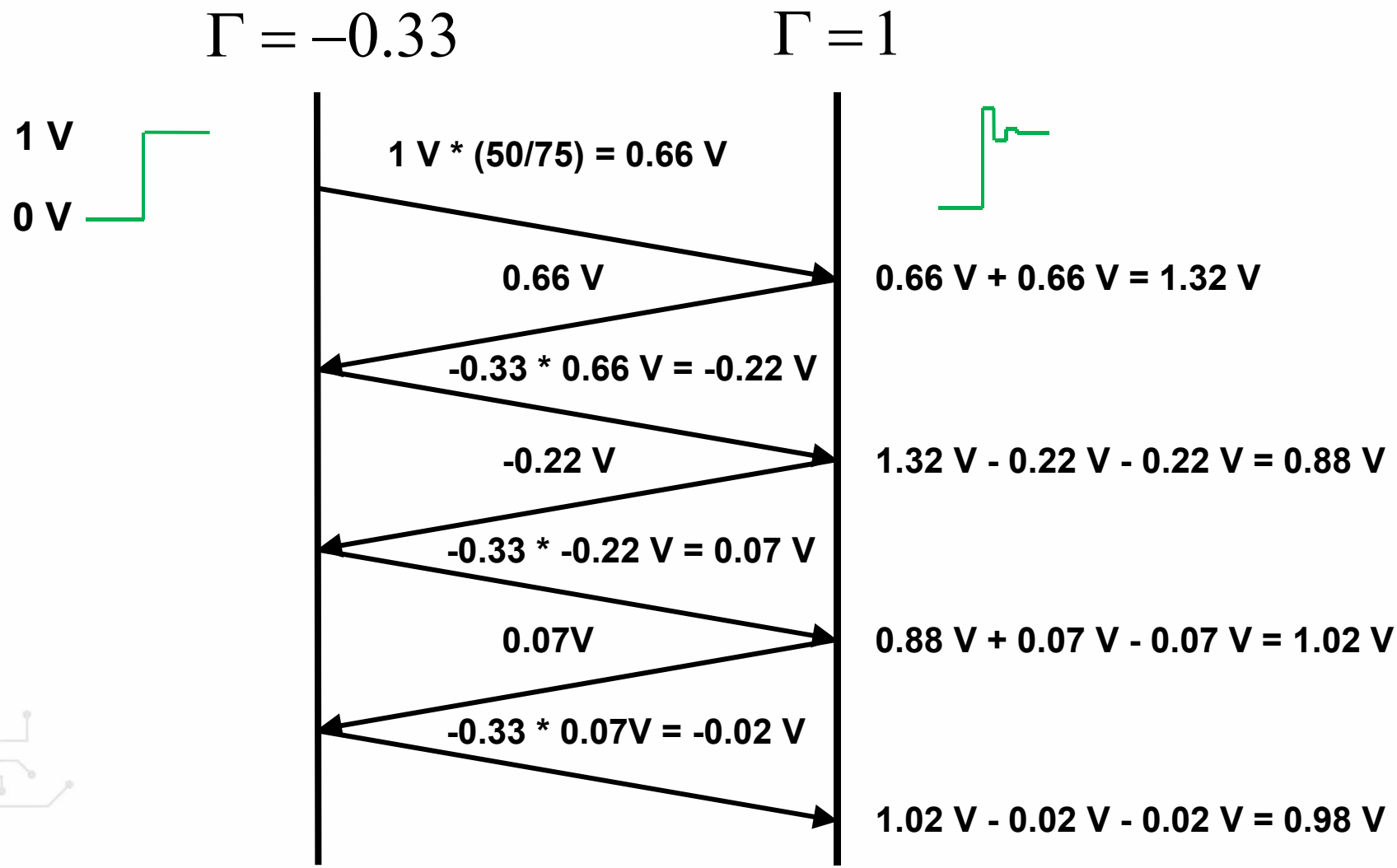
Multiple Reflections: Example



$$\Gamma_{source} = \frac{25-50}{75} = -0.33$$

$$\Gamma_{receiver} = 1$$

Multiple Reflections: Bounce Diagram

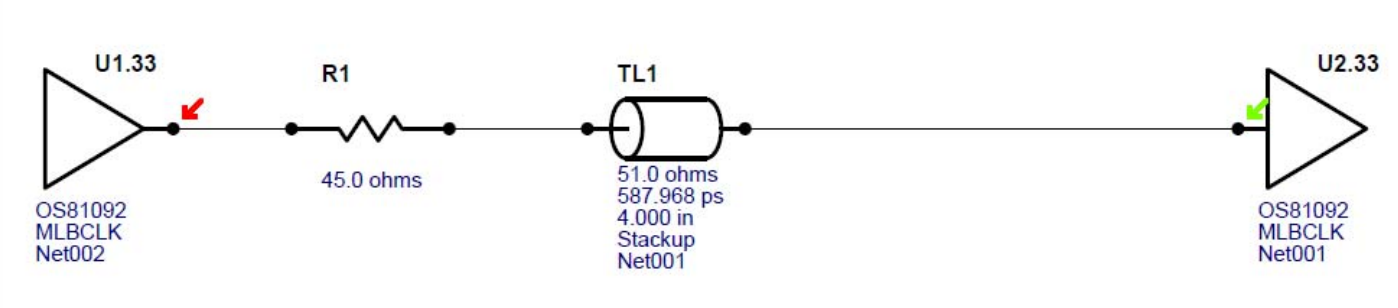


Terminating Transmission Lines

- **Necessary when transmission line propagation time is greater than 20% of the rise/fall time.**
- **There are four fundamental methods of matching/terminating transmission lines**
  - Source series
  - Parallel far-end
  - Thevenin far-end
  - RC far-end
- **Of these, source series termination is generally the most appropriate for MCU based applications**

Source Series Termination

- Match impedance of driver plus series resistance to characteristic impedance of transmission line.

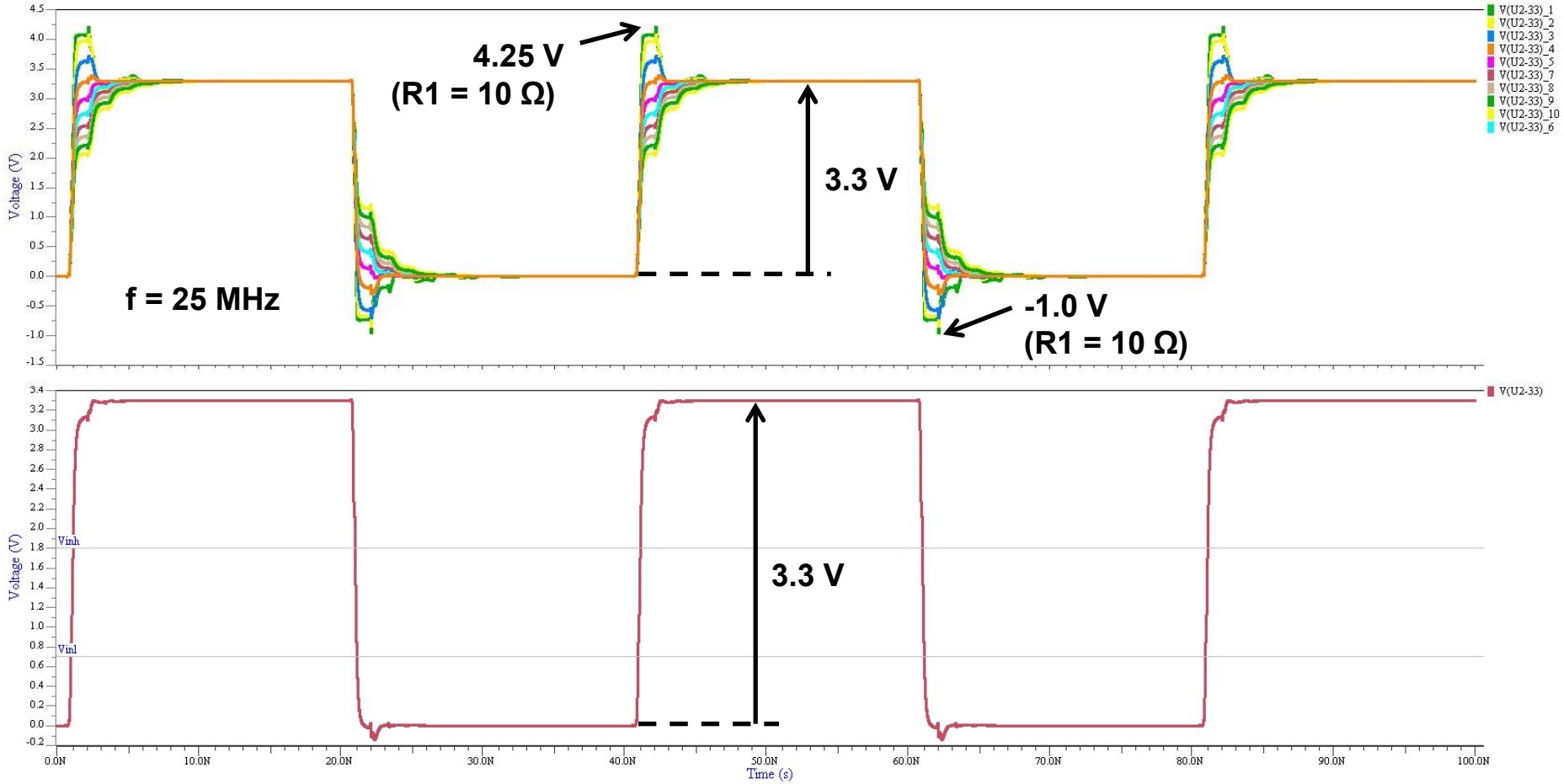


$$R_{Driver} + R_{Series} = Z0_{TL}$$

$$R_{U1} + R1 = Z0_{TL1}$$

Source Series Termination Waveforms

$$R1 = 10 - 100\ \Omega$$



$$R1 = 45\ \Omega$$

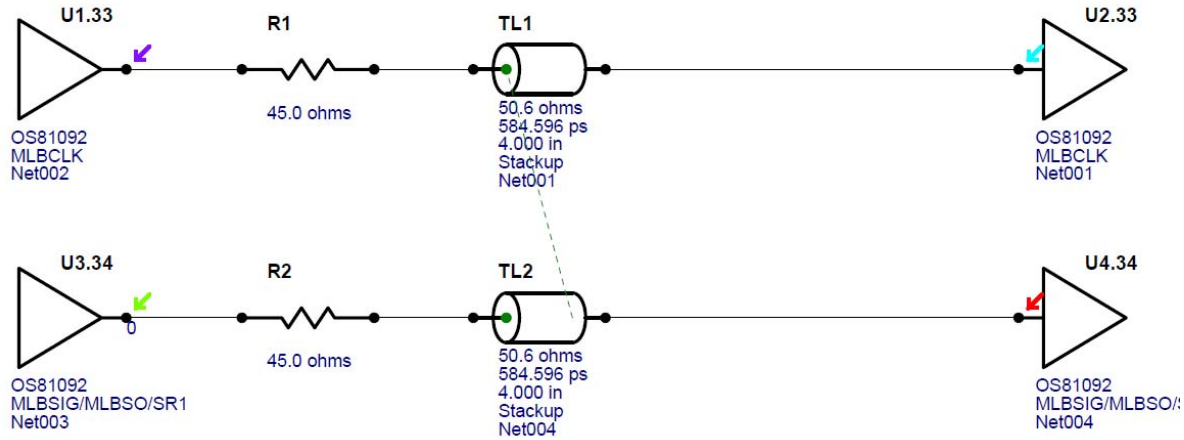
Source Series Termination Guidelines

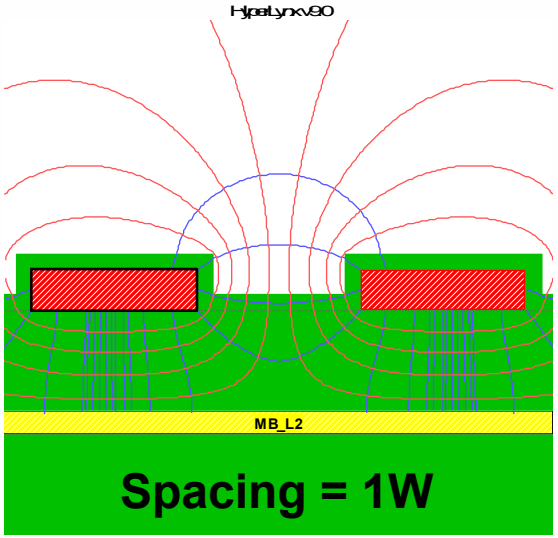
- **Benefits**
  - Only one component required
  - Easy to figure out resistor value
  - Power consumption is low
- **Drawbacks**
  - Increases rise and fall times
  - Full reflection at receiver (may lead to radiated emissions problems).

Crosstalk: Two Lines Model

Aggressor

Victim (driven low)





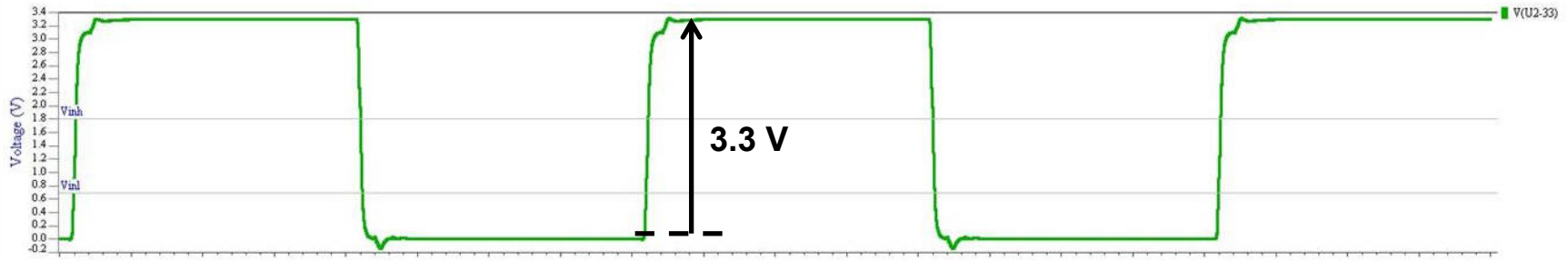
W = width of trace

Note: W = 8 mils for all examples

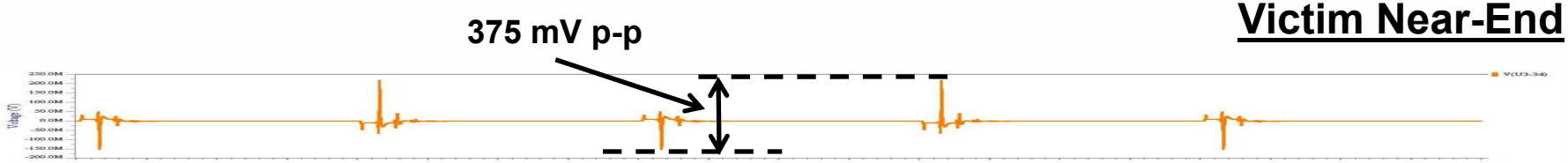
Crosstalk: Two Lines Simulation Result

- Spacing = 1W (Width)

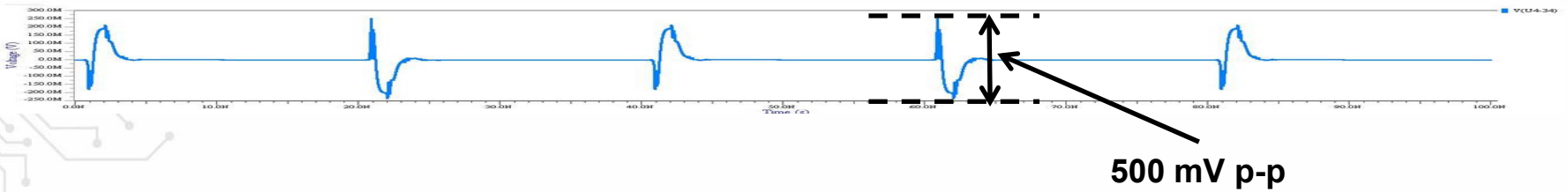
Aggressor Signal



Victim Near-End

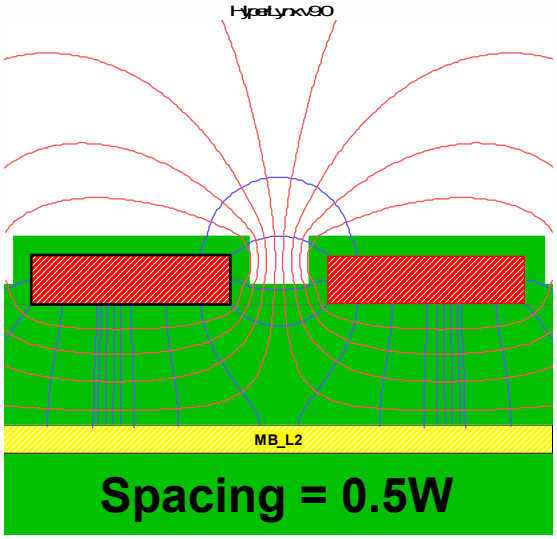


Victim Far-End

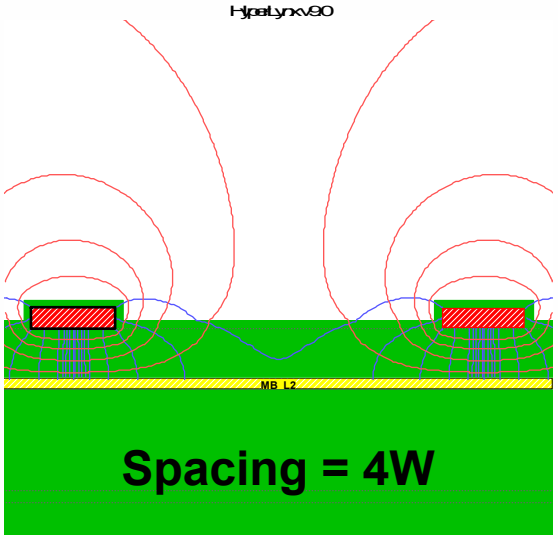


Crosstalk: Two Lines Effect of Spacing PCB Cross-section

- Spacing = 0.5W and 4W



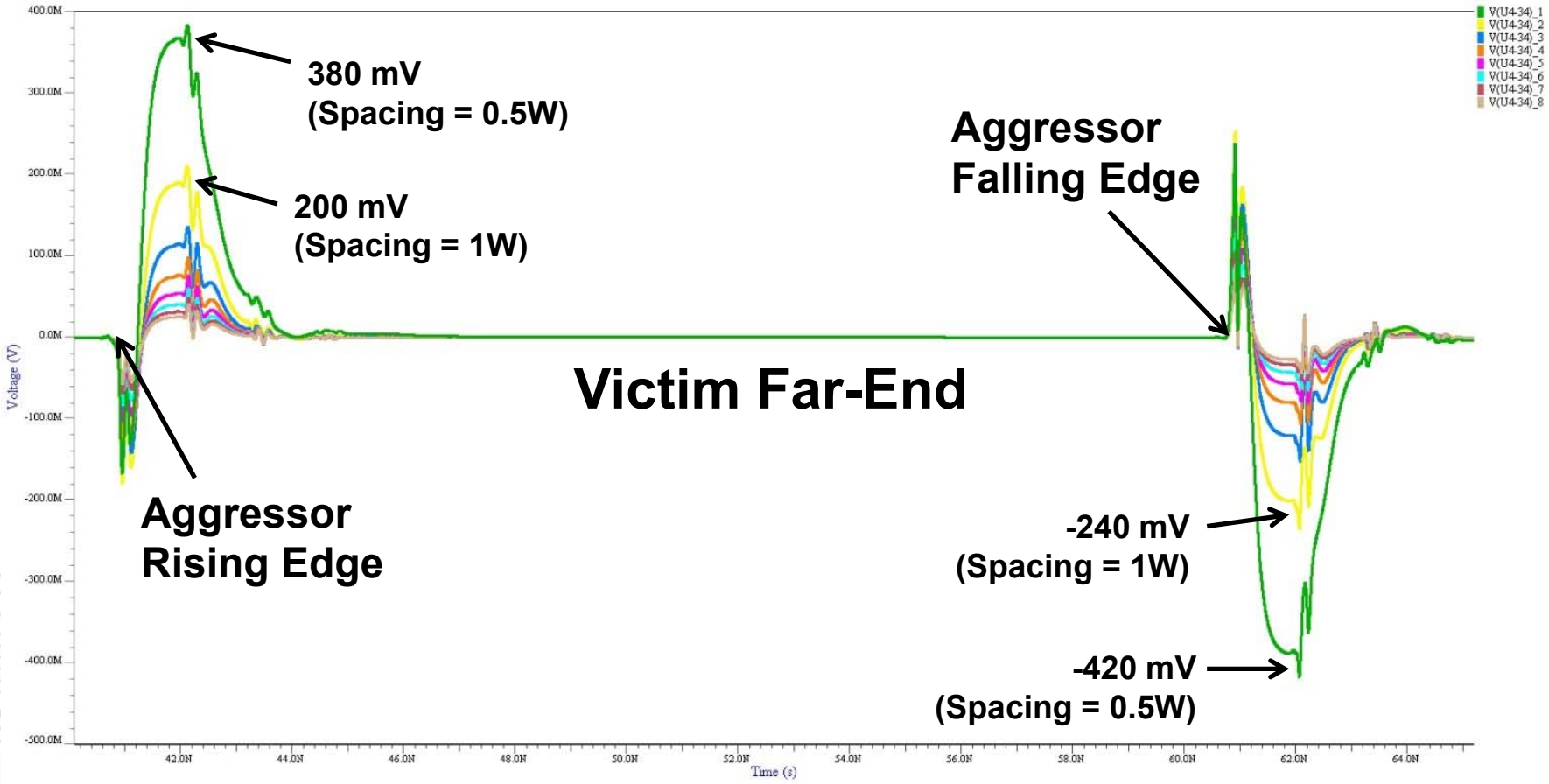
Z_0 = 49.3 Ω



Z_0 = 51.0 Ω

Crosstalk: Two Lines Effect of Spacing Simulation Results

- Spacing = 0.5W to 4W, steps = 0.5W

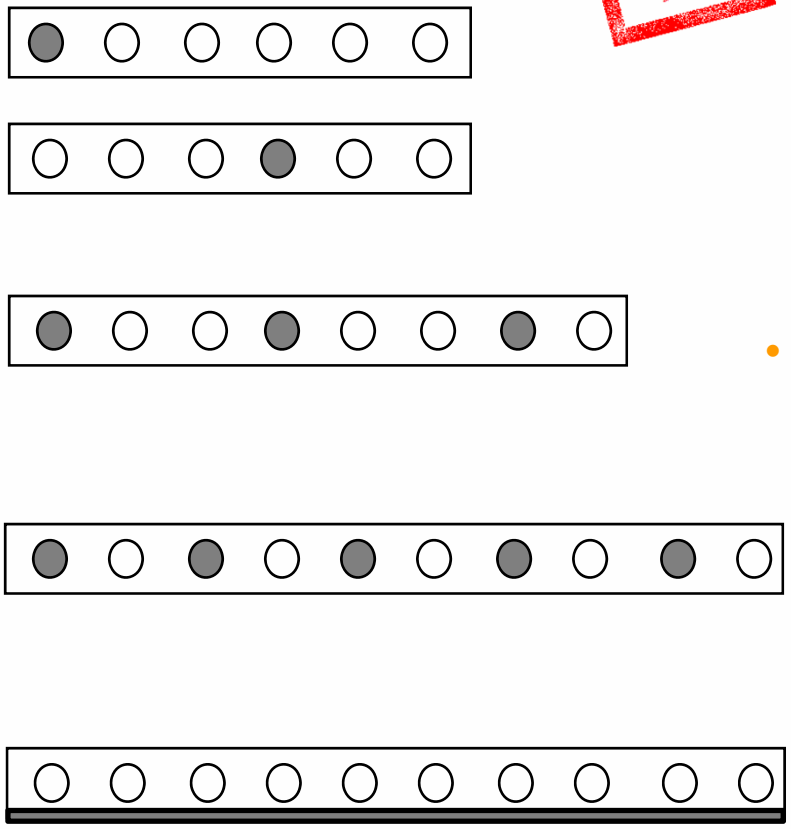


Mitigating Crosstalk

- **Increase space between conductors.**
  - Going from 1W to 3W spacing decreases the far-end cross talk by 65%.
- **Decrease the length of the coupled region by avoiding long parallel routes.**
- **Bury sensitive lines to internal layers.**
- **Add Guard Traces.**

Ribbon Cable and Crosstalk

WORST



BEST

- Large loop areas
- Common impedance (common-mode) coupling
- Crosstalk

- Smaller loop areas
- Some common-mode coupling
- Some crosstalk

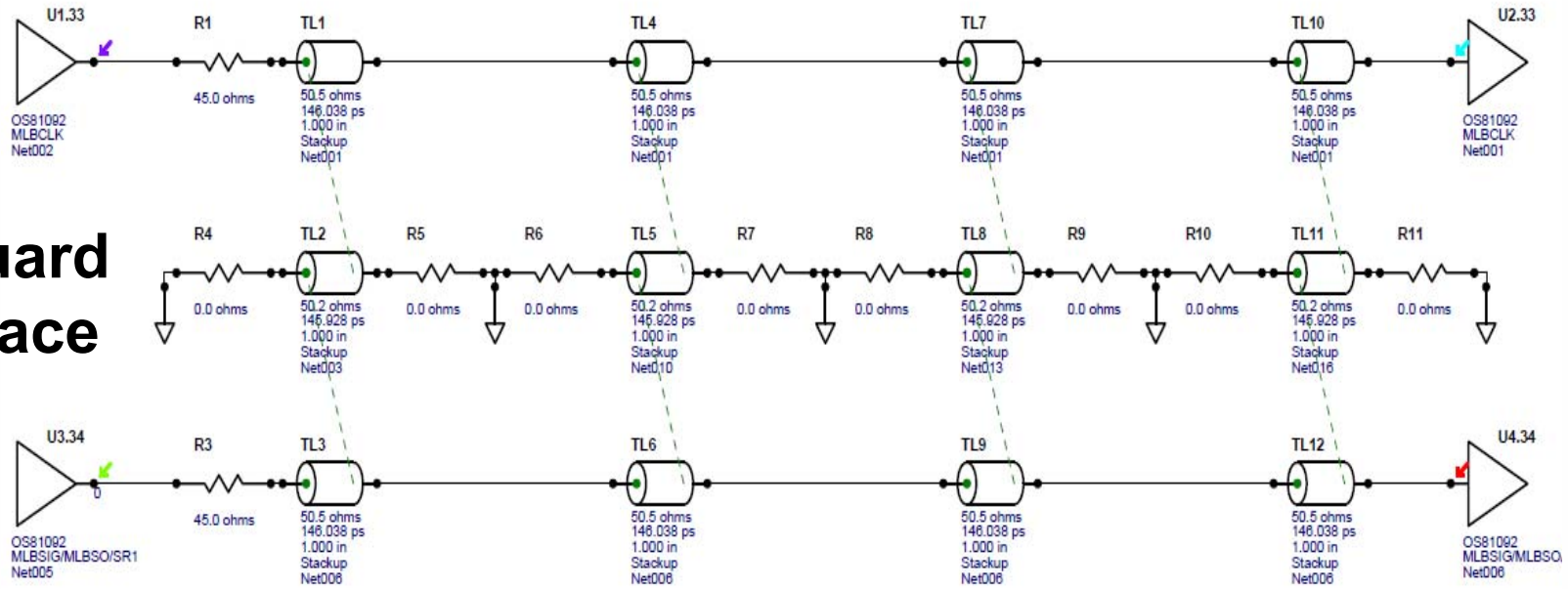
- Very small loop areas
- No common-mode coupling
- Less crosstalk

Grounded Guard Trace: Multiple Ties (PCB) Model

Aggressor

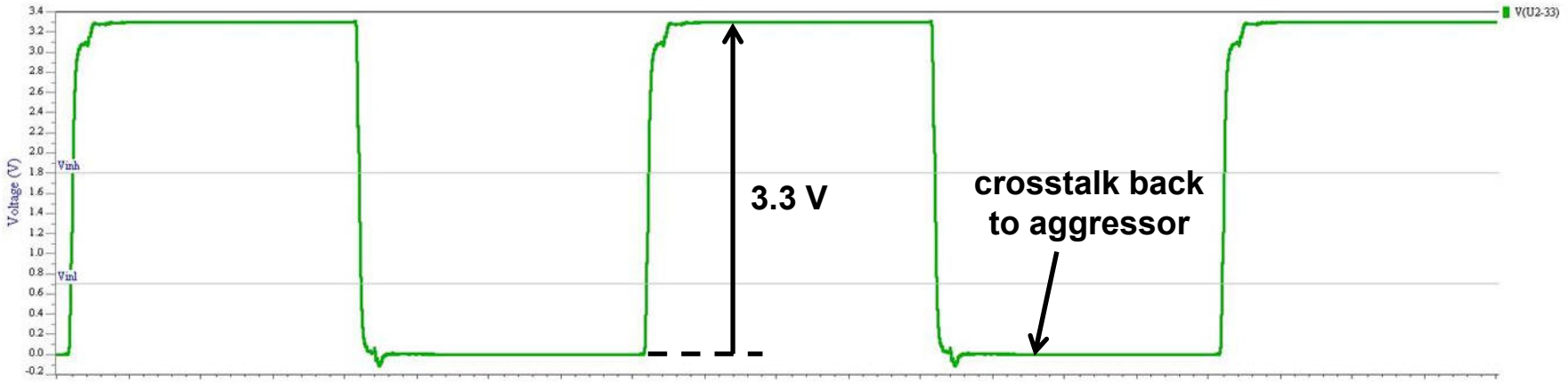
Guard Trace

Victim (driven low)

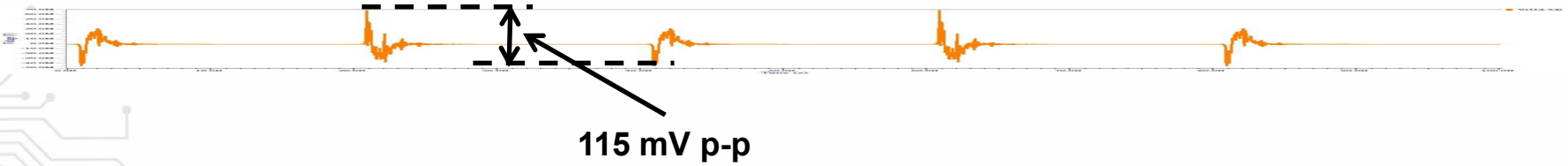


Grounded Guard Trace: Multiple Ties (PCB) Result

Aggressor Signal

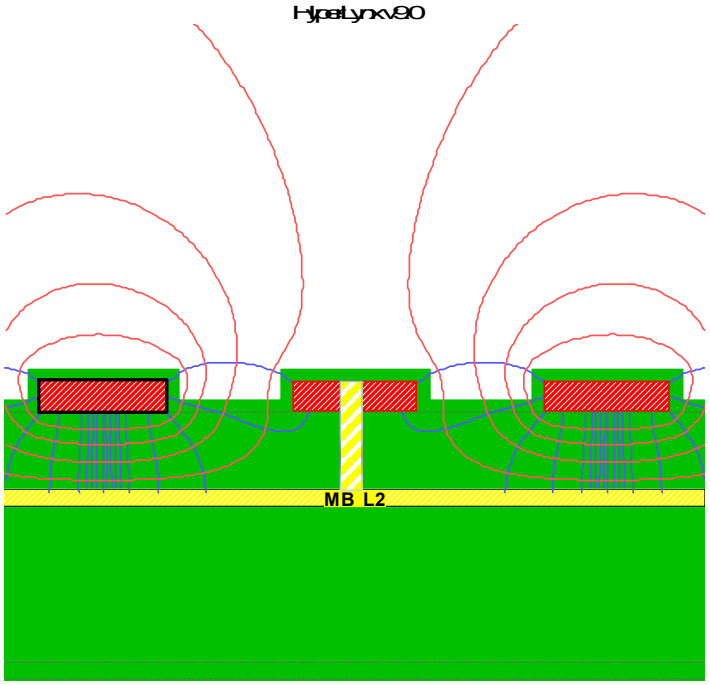


Victim Far-End



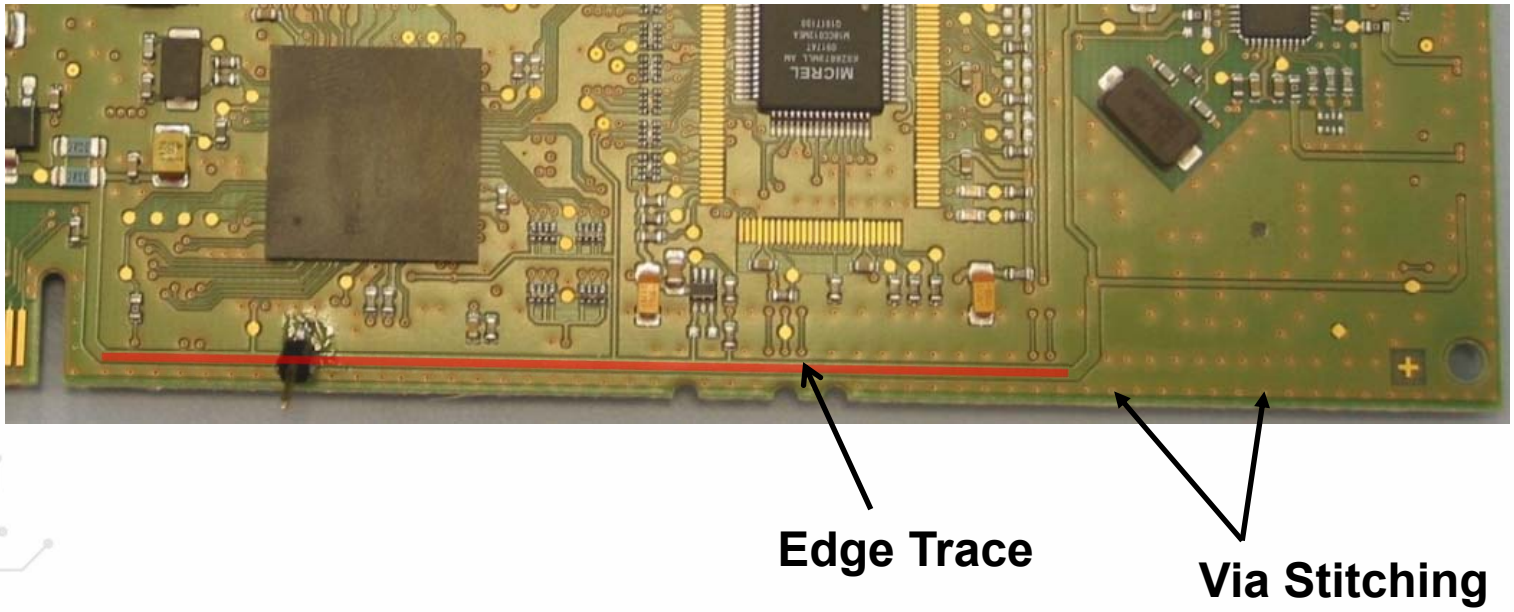
Grounded Guard Trace: Summary

- At a **minimum** ground guard traces at both ends
- For **best results** add as many ground taps as possible



Grounding schemes and isolation techniques

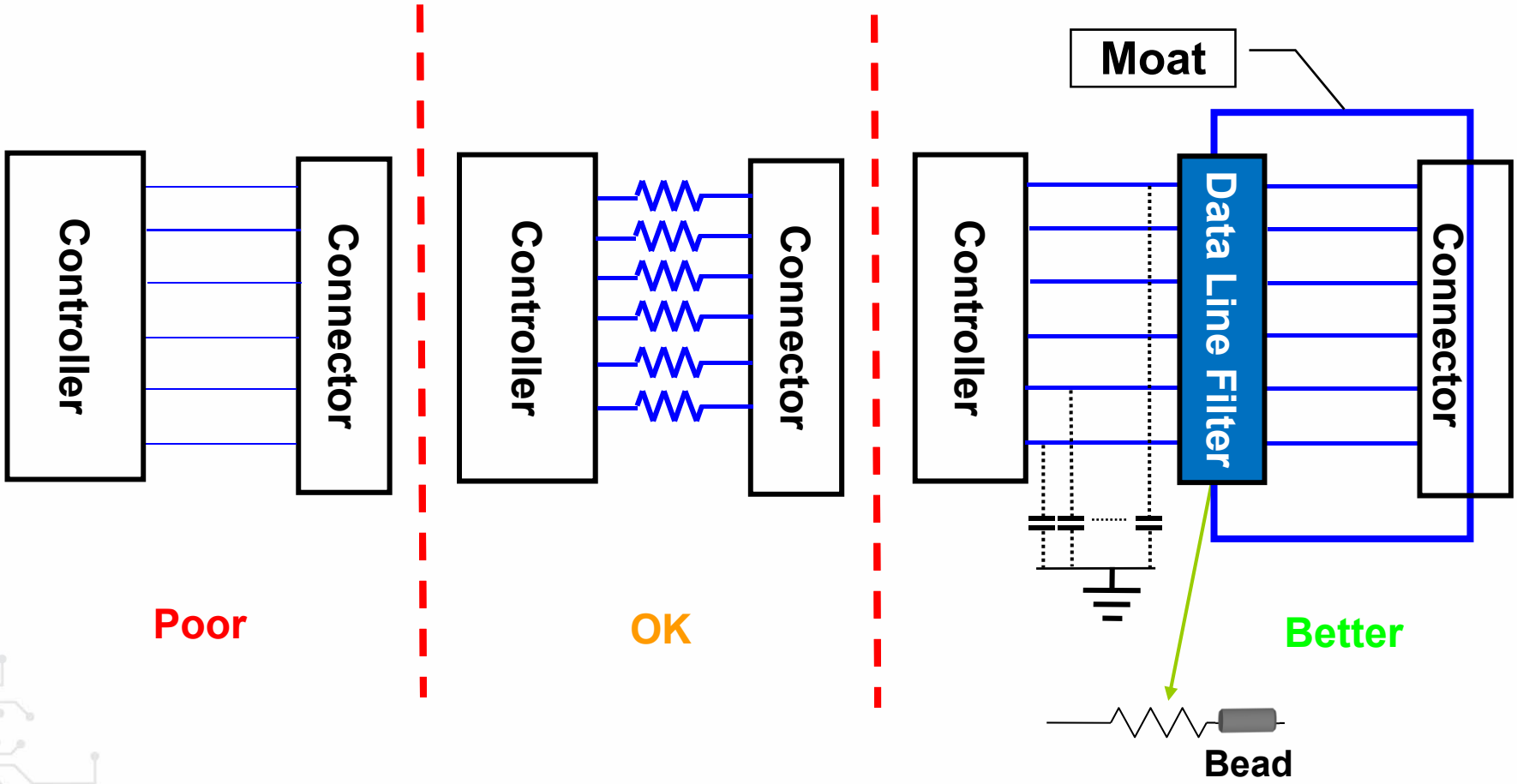
- **Trace routed near board edge**
  - Return stitching vias near board edge should reduce board edge radiation (low potential for root cause)



Agenda

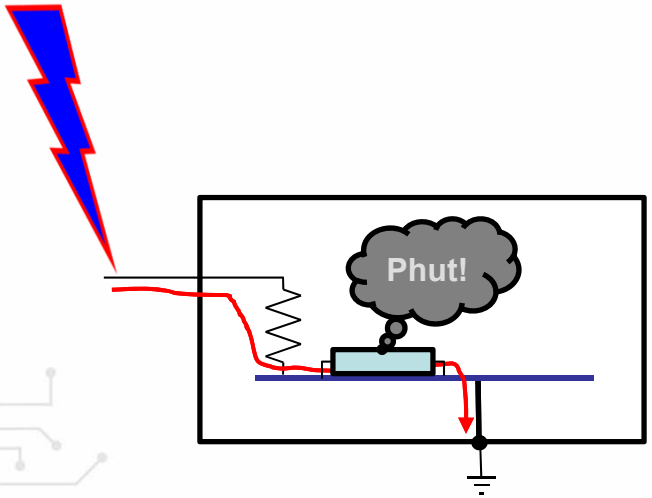
- What is ‘EMC’ and Why We Care About It
- Characteristics, Quantification and Radiation Modes of Electrical Noise
- Noise Path Control
- Signal Integrity
- **Design for EMC**
  - Circuit Design for EMC
  - PCB Design for EMC
- Real-Life EMC ‘uh-ohs’!
- EMC Guideline Summary (reference)

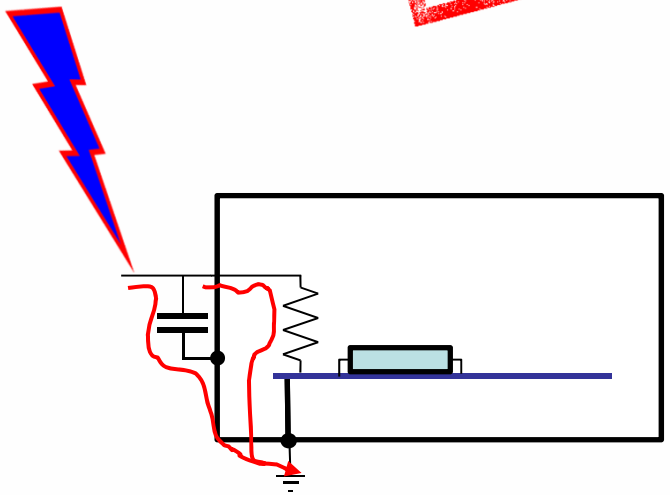
PCB Connector Isolation



Keeping the Noise Out

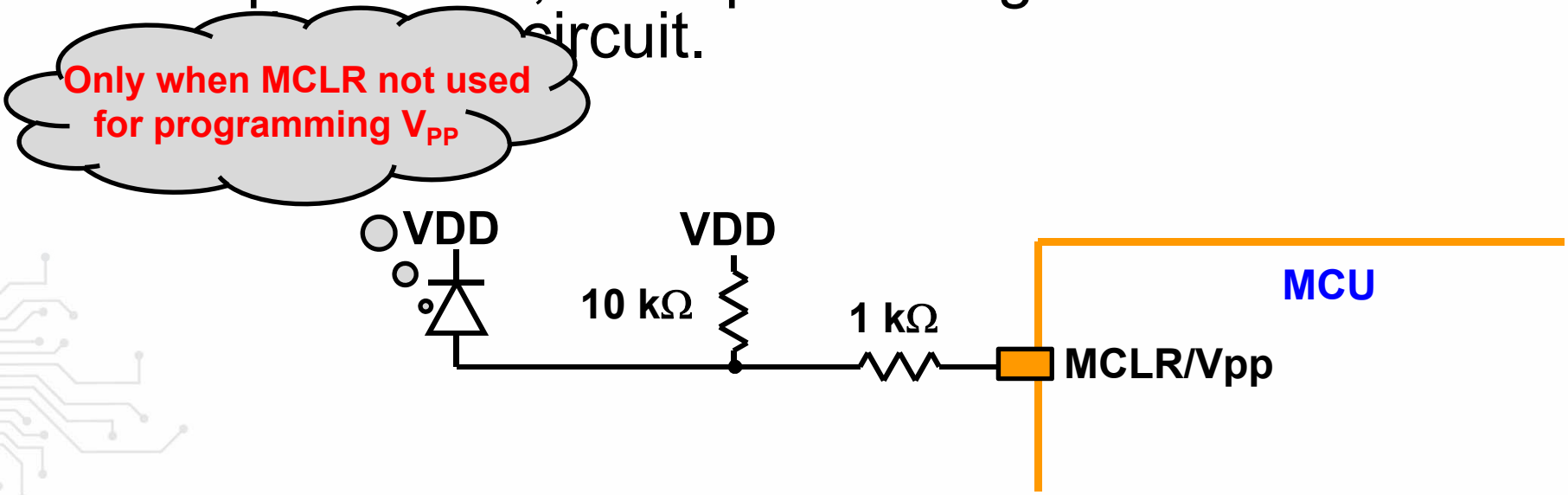
- **If possible, bond incoming signal shields and/or filters to chassis not PCB**
  - Provide low-Z path for incoming EMI away from sensitive circuitry
  - Consider moat isolation on PCB





Safe Handling of the MCU Reset Pin

- **Reset/MCLR Pins**
  - Series resistor to limit the amount of current entering the MCLR pin during ESD/EOS event
  - Add diode to VDD for additional ESD protection, if not performing ICSP™ of the circuit.



Application Circuit Design for EMC (1)

- Select the most up to date technology devices suitable for the task.
- Operate at the slowest clock speed practical to achieve goal.
  - Reduced Idd transient current peaks and frequency
  - Reduced susceptibility bandwidth to external noise
  - Reduced effective emissions bandwidth

- **The above applies to all devices within an application!**

Application Circuit Design for EMC (2)

- For device I/O:
  - Terminate all unused inputs
  - Avoid sharing clocks between devices
  - Use slew rate control for outputs
  - Use differential signals (CAN, LVDS, …) wherever practical
  - Decouple appropriately and adequately, including all I/O to RF (chassis) ground if possible
  - Place series resistors at MCU end of all port input traces that go off board (e.g. keyboard) for ESD

Application Firmware: Immunity Improvement

- Debounce input signals
- Filter and clamp A/D converter results to avoid unforeseen out of range issues
- Periodically reinitialize SFRs and I/O port direction and remapping configuration (Peripheral Pin Select) if supported
- Protect critical data
  - Flash vs. EEPROM
  - CRC, parity, ECC or redundancy

Application Firmware: Immunity Recovery

- Fill unused Flash with software reset instruction
- Populate all unused vectors with reset address
- Utilize device's functional safety features:
  - Watchdog/Windowed Watchdog Timer
  - Uninitialized register, oscillator fail, address & arithmetic error, uncorrectable Flash ECC error exceptions
  - Class B library
    - www.microchip.com/classb

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  - PCB Design for EMC
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PCB Layout Objectives

- **Minimize the radiated (differential and common mode) and conducted emissions:**
  - from and within the system/PCB
  - from the I/O and other cables connected to the system/PCB
- **Isolate sources of noise (internal and external) from susceptible areas of the system/PCB**

A lower level of emissions will tend to also result in improved immunity

Radiation Potential

- **The radiation potential of a PCB in a system is a direct function of:**
  - The trace and cable length (common mode current flowing on them)
  - The loop area encompassed by the signal and its return path (differential mode currents on them)
  - The HF spectral content of the signal they are carrying

High Threat Signals (1) (Emissions)

- **High threat signals** have any or all of the following characteristics
  - High frequency
  - Fast rise and/or fall time
  - Large voltage swing
  - Large switching currents
- The high threat signals should be identified and given priority before finalizing power distribution network (PDN)
- **Signal traces should be kept as short as possible** (to control common mode emissions)
- **Signal loop areas should be minimized** (to control differential mode emissions)

High Threat Signals (2) (Emissions)

- **Control trace characteristic impedance for all High Threat signals and terminate appropriately**
- **Other points to consider:**
  - The signal harmonic content, not just the fundamental
  - Signal integrity: at high frequencies, even short trace lengths can effect signal integrity
  - Isolate High Threat signals from sensitive traces/circuit areas
  - Keep High Threat signals away from PCB edge and connectors

Highly Threatened Signals (Susceptibility)

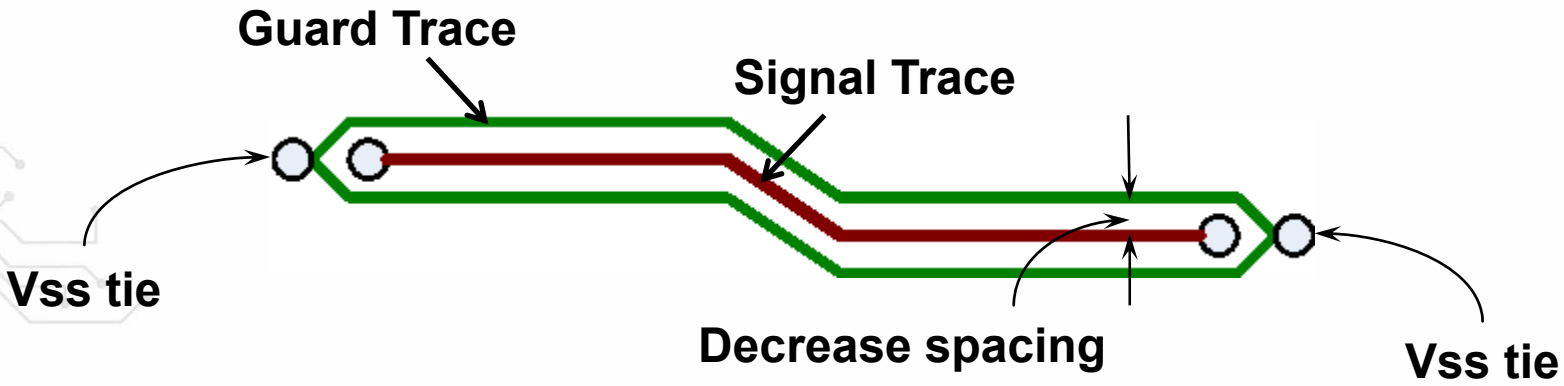
- Signals which are susceptible to E-M noise include:
  - Oscillator circuitry/PLL
  - Interrupts
  - Reset/MCLR
  - Any edge sensitive inputs (without a low-Z tie to either Vdd or Vss)
  - Any wired-OR signals
  - Any high impedance source like sensors or drivers

Key Principle for PCB Design Success!

- **Don't think of 'ground' as a place current goes, think of it in terms of a 'current return path' (Kirchhoff's Law)!**
- **Consequently, signal return current flowing through a 'ground' plane:**
  - Contains the same fundamental and harmonics as the signal
  - Responds to all circuit components, real or parasitic, within the total loop
- **Key principle:**
  - Always identify and provide a low Z signal return path back to the signal source
    (signal will find the lowest Z return path in any event which may not be the best for EMC)

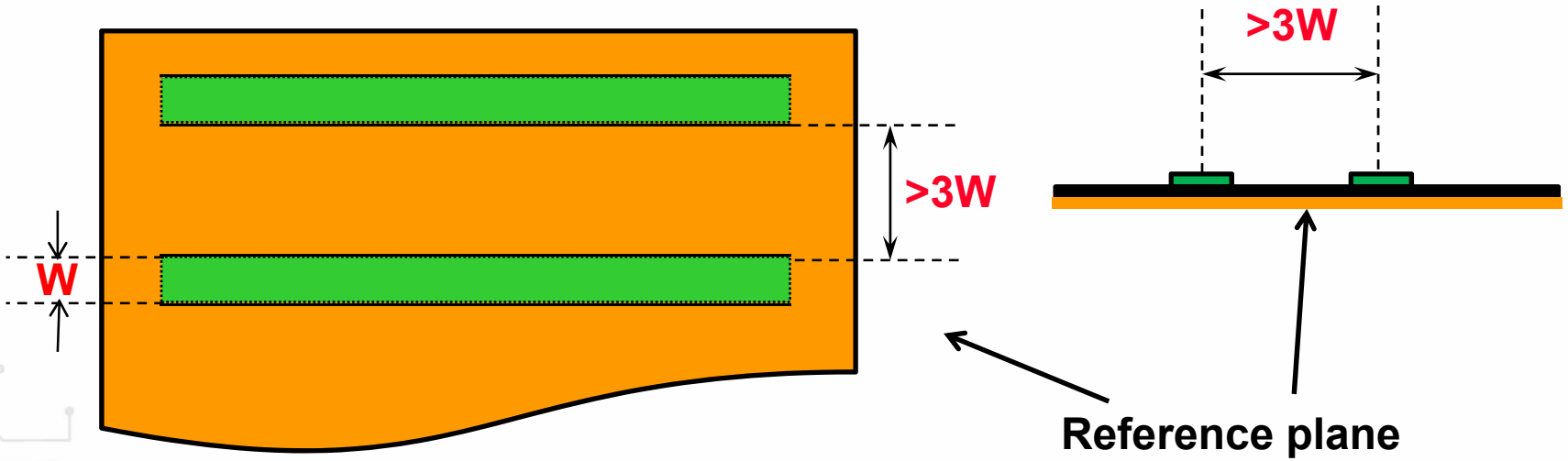
Guard Traces

- **Guard traces for high threat or highly threatened signals:**
  - Keep total loop area down
  - Help control signal trace impedance
  - Are ideally suited to one and two layer PCBs
- **Avoid sharing guard traces with more than one signal trace. Always tie to Vss at each end (at least, esp. for HF signals)**
- **Two layer example – no return (Vss) plane**



Trace Spacing

- **The 3-W Rule reduces the impact of high threat signals**
  - Represents the 70% flux density boundary
  - Removes the need for a guard trace in most applications

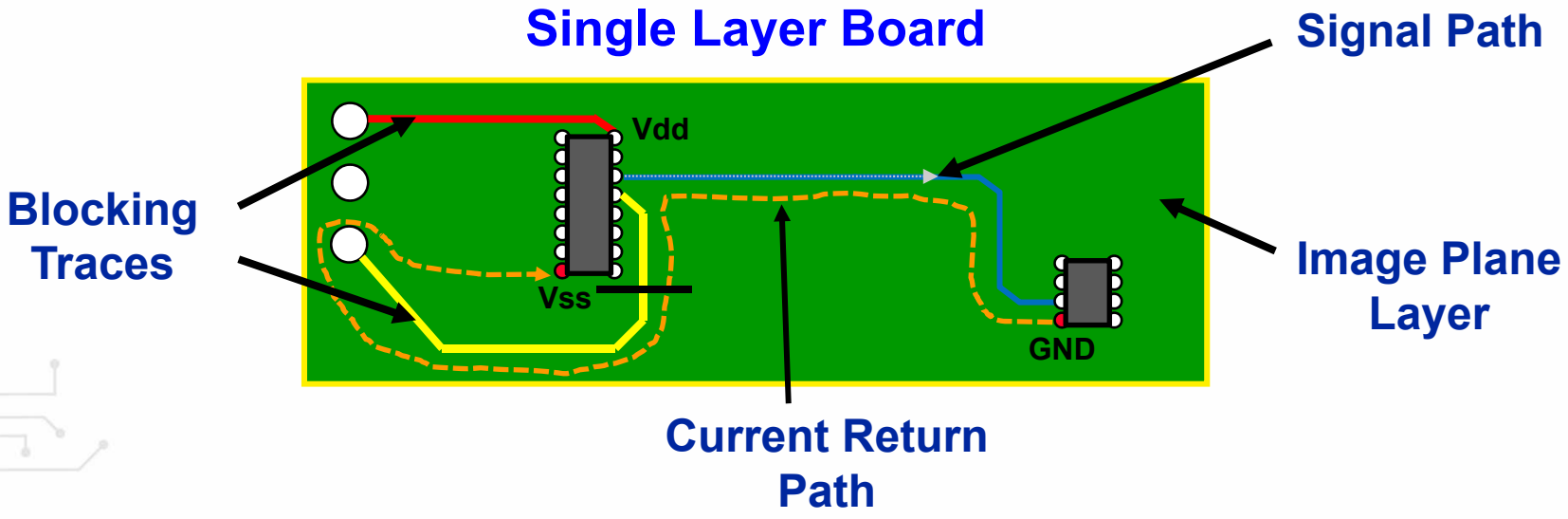


The Image Plane

- **An image (or reference) plane provides an optimal return path back to the source for RF currents, reducing crosstalk and emissions.**
- **It can be a:**
  - Ground plane
  - Power plane
  - Isolated layer
  - Chassis
- **No signal traces should be present on an image plane**
- **Too many through hole components can destroy the integrity of an image plane**

Implications of a Discontinuous Image Plane

- Placing signal traces within an image plane layer can introduce large loop areas resulting in a higher return path impedance (and emissions)
- This applies to the return paths of the signals within the image plane, and signals in other layers



PCB Inductance

- Significant source of return path noise

$$V_{noise} = L \frac{di}{dt} \text{ Volts}$$

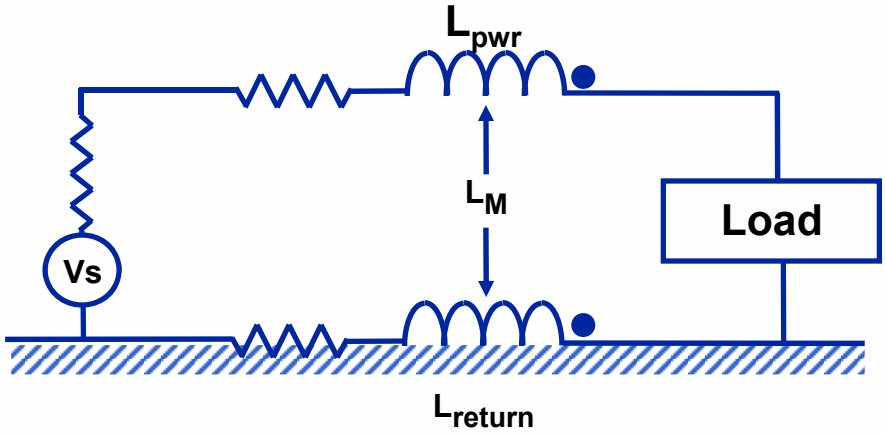
- For a trace above an image plane

$$L = 0.005 \ln(2\pi H/W) \text{ uH/in}$$

- For a current loop (e.g. power & return/'ground')

$$L = L_{pwr} + L_{return} - 2M$$ (M=mutual inductance)

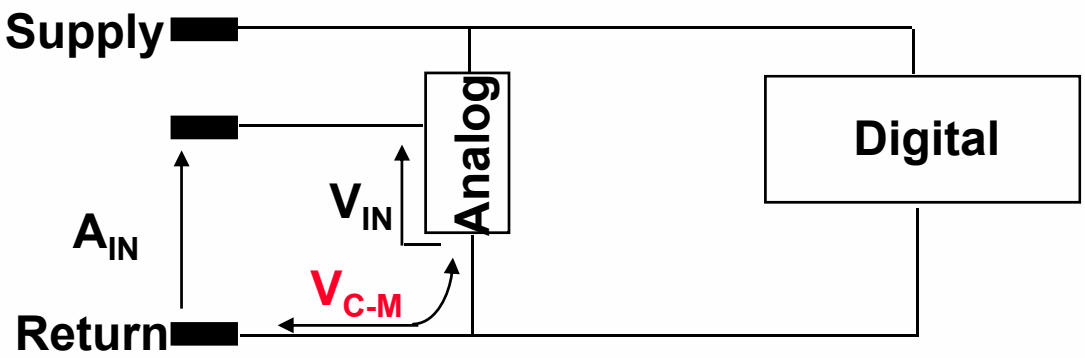
- Reduce Noise by reducing L
  - ↓ H (height above return path)
  - ↑ W (width of trace)



Common Impedance Coupling

- **Common-impedance (common-mode) coupling:**
  - The unwanted coupling of signals using a shared return path
  - Proportional to the current return path impedance
- **Can introduce digital noise into sensitive analog or interface subsystems**
- **Can cause RF noise to couple onto external ports**
- **Can cause unwanted coupling between signals within a circuit**
- **Mitigated by the elimination of the shared return path (or at least reducing the shared return path impedance)**
  - Partitioning and use of a single point (lowest Z) return
  - PCB isolation though techniques like ‘moating’

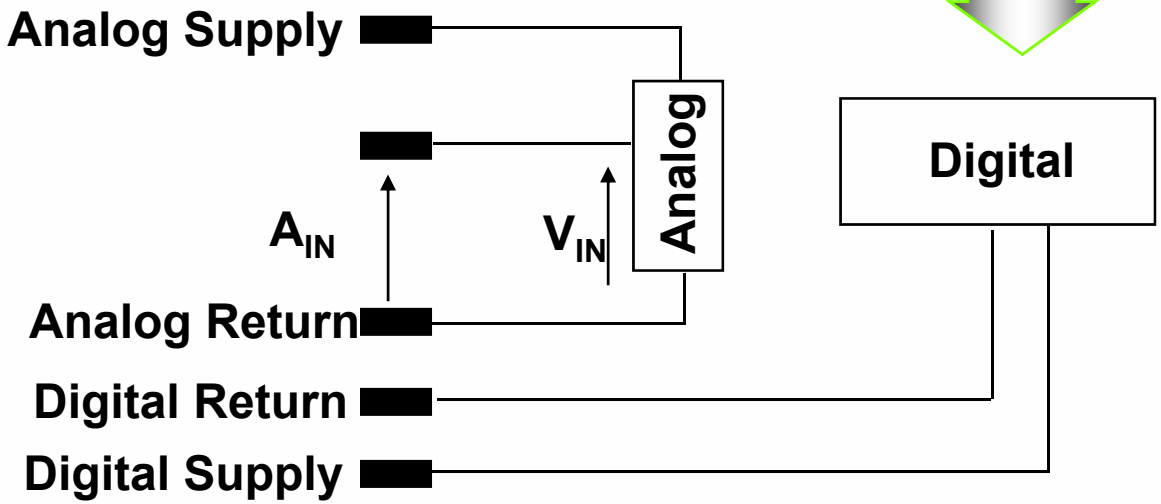
A Common Return: Analog in a Digital Environment



Poor Scheme

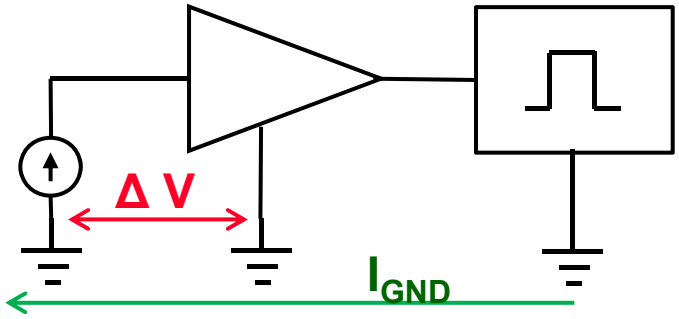
$V_{IN} = A_{IN} +/- V_{C-M}$

Better Scheme

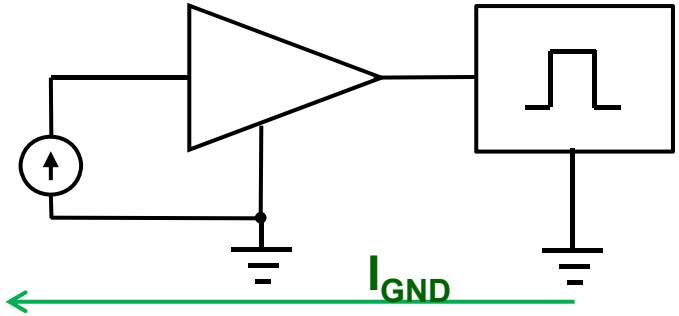


Returns Connected to a Single Point (power supply lowest impedance return point)

Sensor input

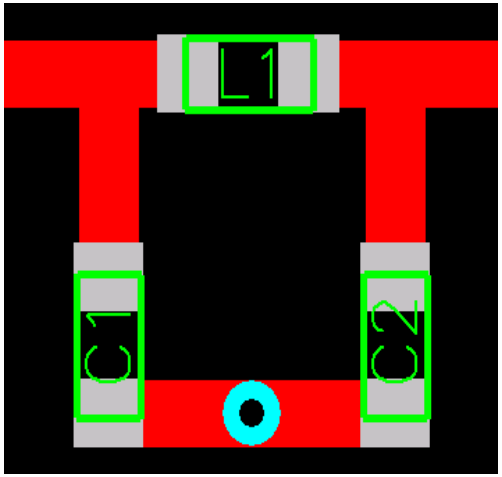


Bad

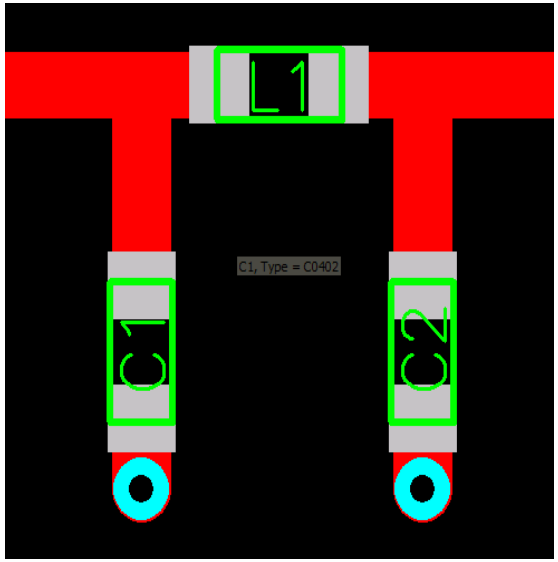


Good

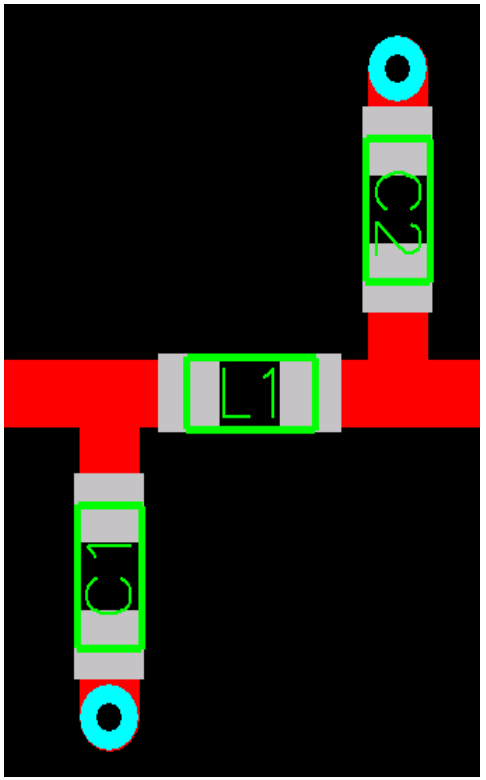
Coupling within a Pi-Filter



Poor
(potential common-mode and crosstalk coupling)



Better
(potential for crosstalk coupling)

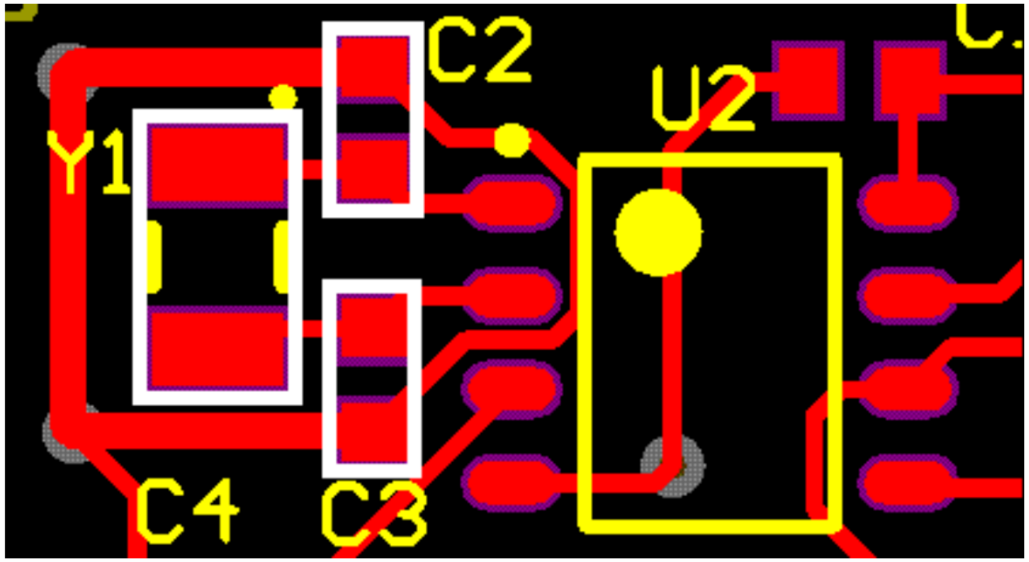


Best
(all coupling minimized)

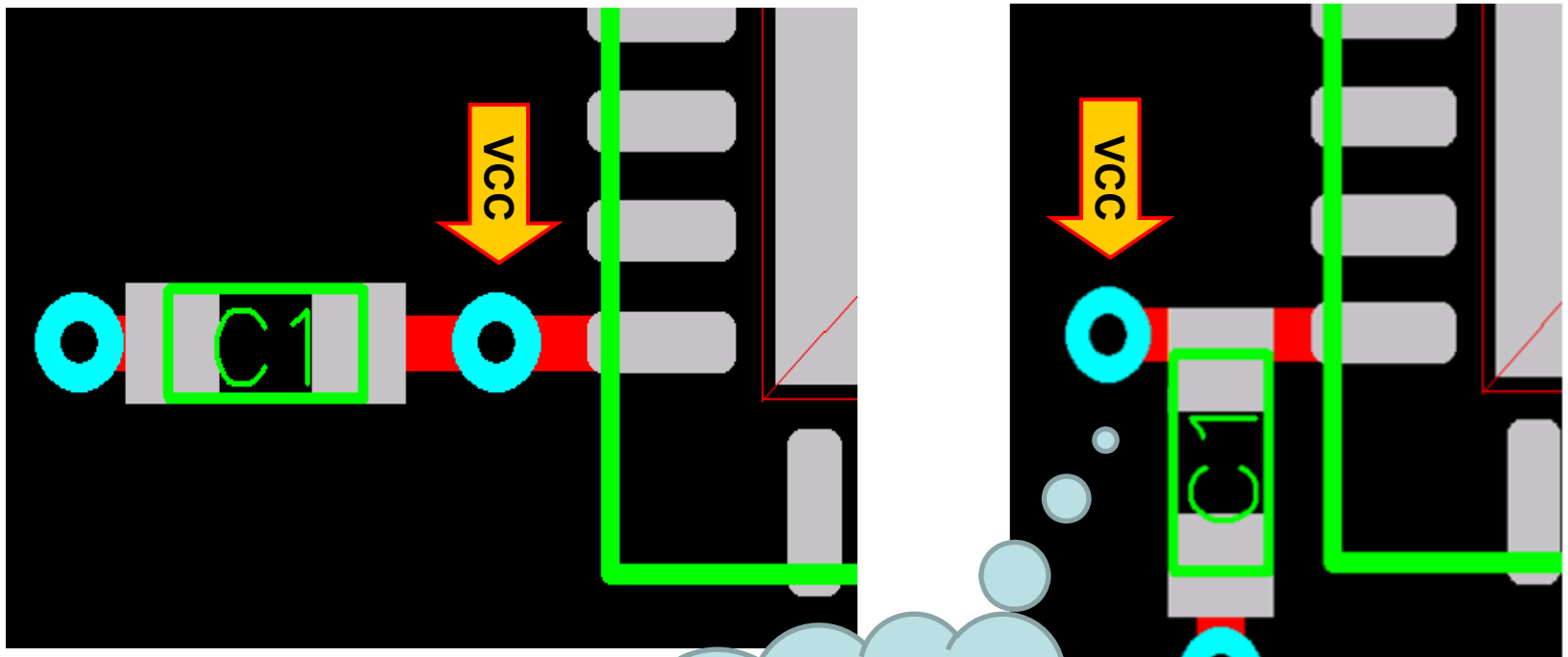
MCU Oscillator Layout

- **Crystal oscillators are potentially both susceptible and noisy**
  - Circuit must be contained close to the device
  - No unrelated trace must run across or close by the oscillator network(s)

Tie to closest MCU ground!



VCC Decoupling



Tie to power plane after decoupling

Poor

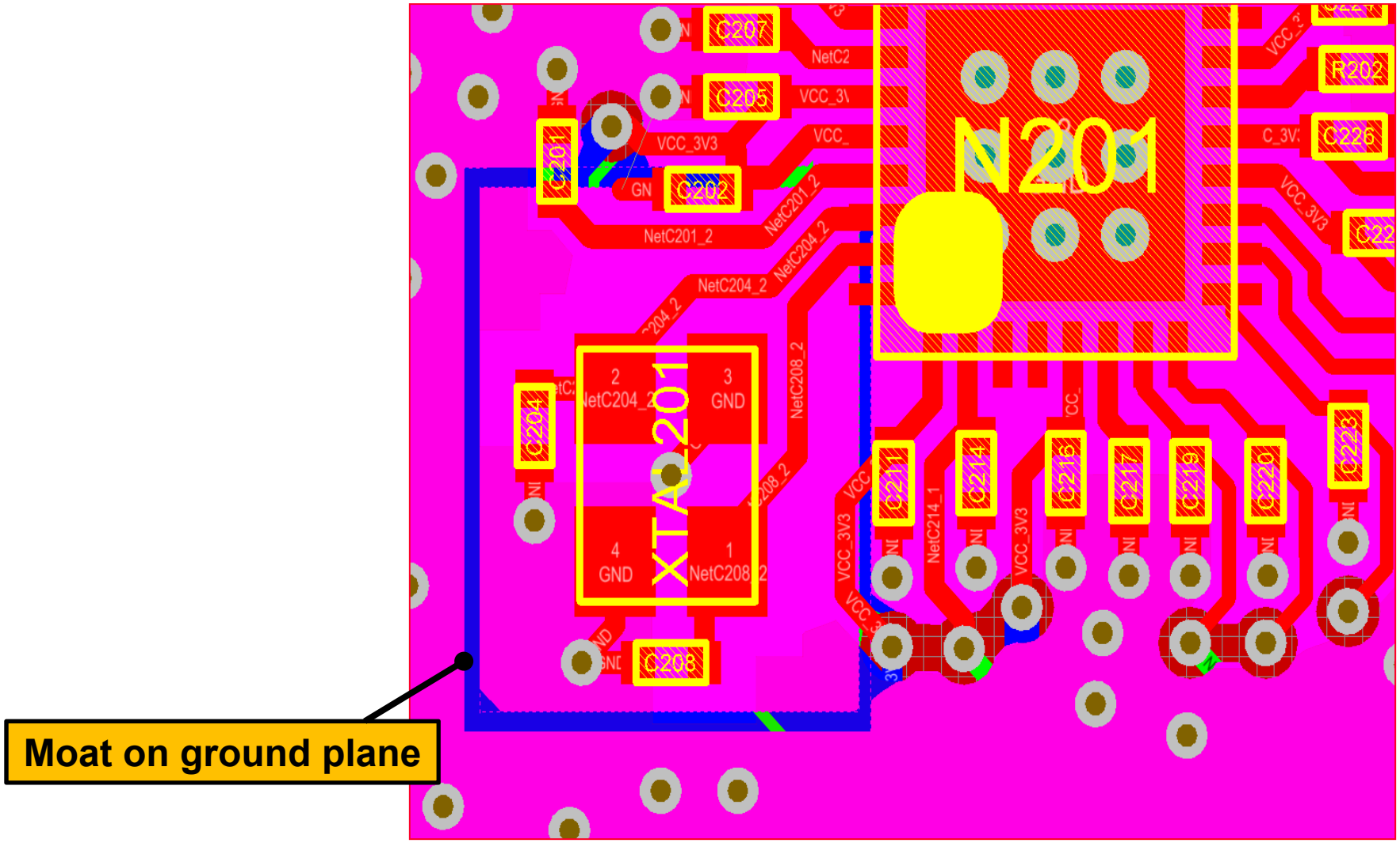
Good

Digital/Analog Isolation

- **Common-mode coupling should be avoided by partitioning (as discussed) and isolation**
- **Isolation is easiest to obtain through a technique referred to as "moating"**
  - Establish a 50 mil wide "moat" surrounding the area to be isolated
  - Remove copper in moat on all planes
  - Use a single "bridge" to funnel signal & power across a common return plane
  - Do not cross the moat with any signal or power traces
  - Bridge should be tied to chassis (or lowest Z supply return point) on both sides
  - Power trace(s) should be filtered with a ferrite across the bridge
    - Signal traces may also be filtered using a ferrite if necessary

Moats keep intruders away

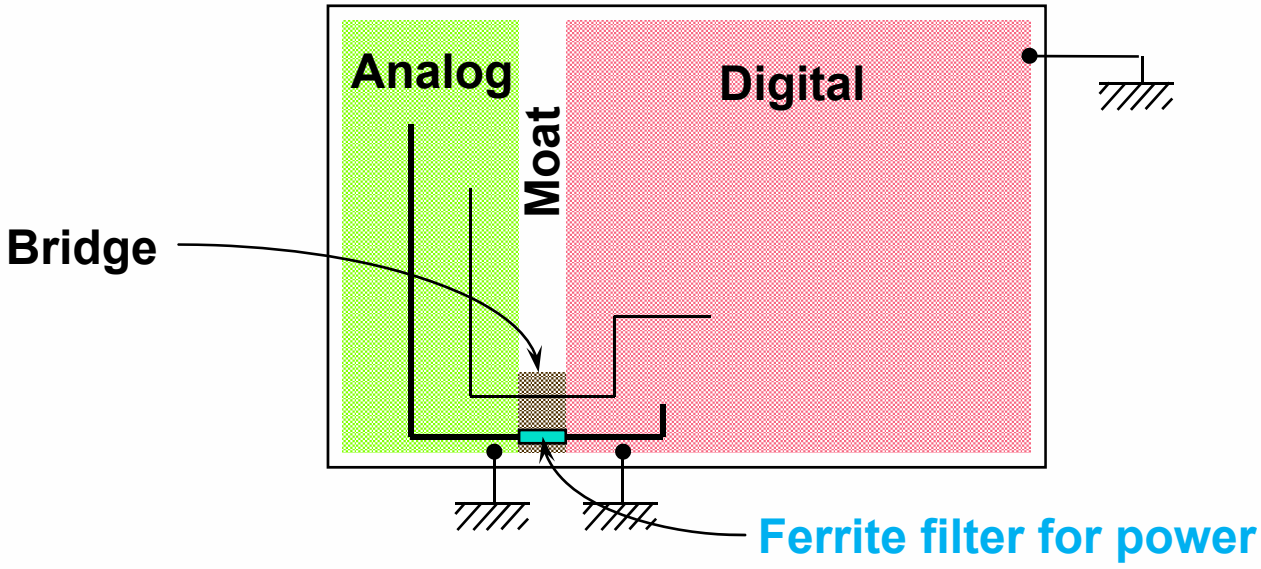
Moat on the ground plane



Digital/Analog Isolation Example

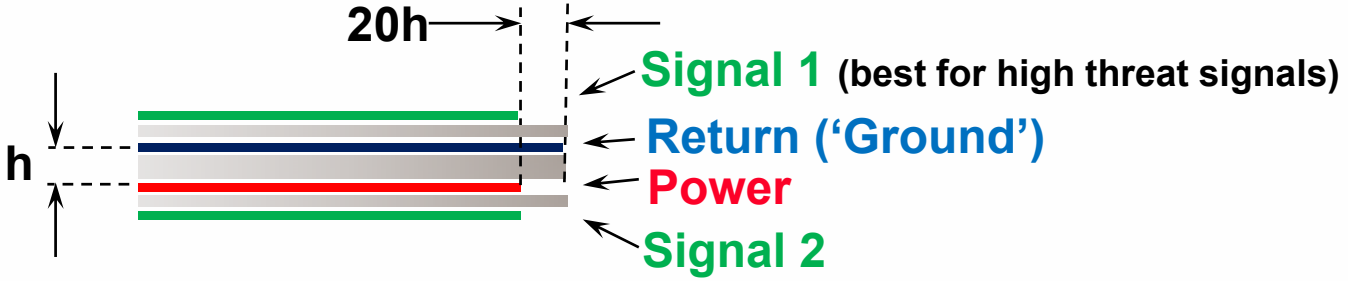
- Moat substantially isolates the analog reference plane from digital noise
- Analog Vss and digital Vss should be separated by the moat only if supported by the analog device
- If no signals > 5 kHz need to cross the moat, remove the bridge and tie A_{vss} to D_{vss} with a ferrite
- For multilayer PCBs, apply “20h Rule” on both sides of the moat between power & return planes

All signals between Analog and Digital sections must only cross via bridge



Multi-layer PCBs

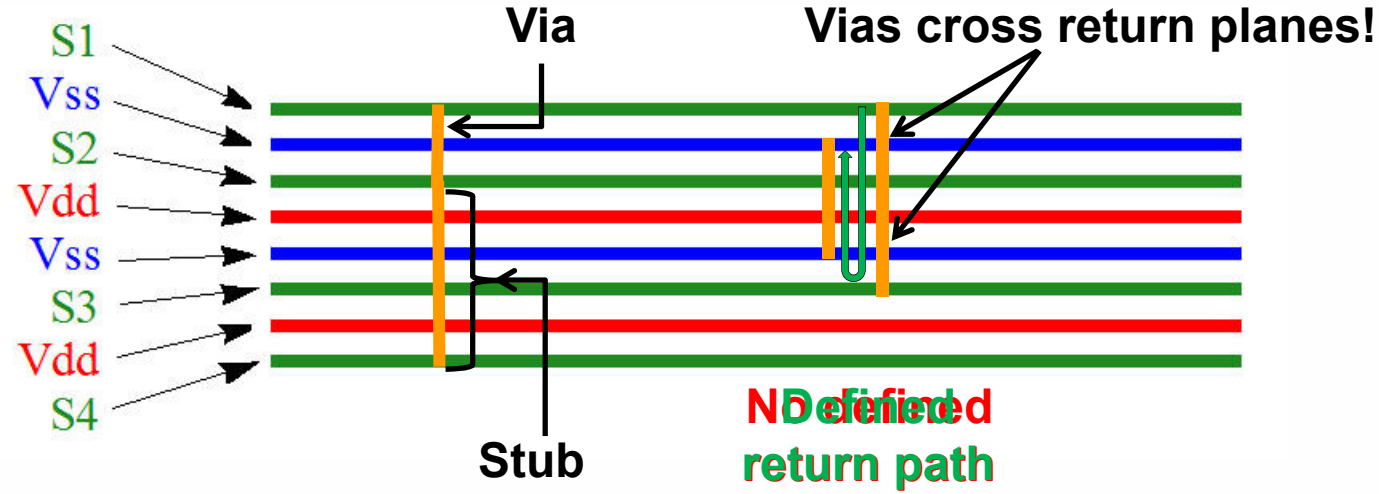
- **Multi-layer boards can significantly help reduce EMC problems if used correctly. They:**
  - Reduce signal trace inductance
  - Reduce total loop areas
  - Simplify routing
  - Increase power supply decoupling
- **The "20h Rule" reduces RF fringing effects (~70%) by extending the return ('ground') plane beyond power plane by 20 times the height between them.**
- **A typical stack for a simple 4-layer PCB is:**



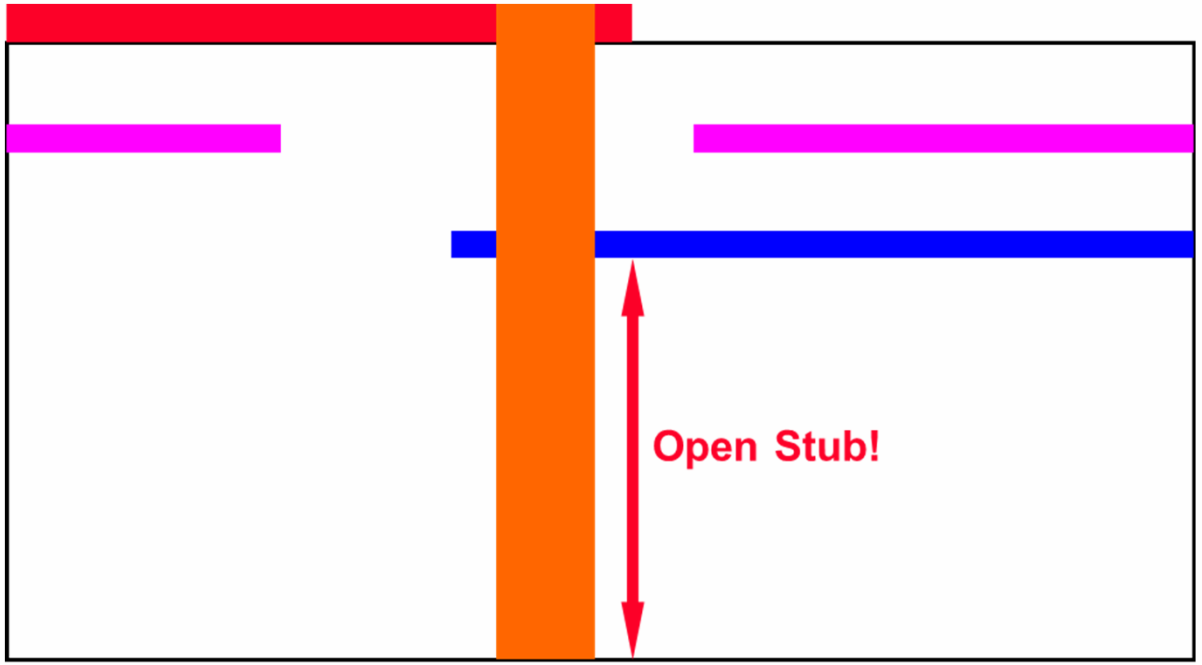
Minimize signal plane dielectric height to reduce trace characteristic impedance for better EMC

PCB Vias

- **PCB vias are inevitable in most designs but act as impedance discontinuities**
  - Minimize use in controlled Z interconnects
- **Via stubs can introduce significant discontinuities for HF interconnects. For these signals consider the following:**
  - Avoid stubs by designing PCB to only using top to bottom layer vias (or vias between close to top/bottom planes)
  - Use buried (blind) vias, or back drill vias that create stubs
  - Avoid crossing return planes with a via. If necessary, provide a via between return planes to define current return path



Open Stub formed by a via

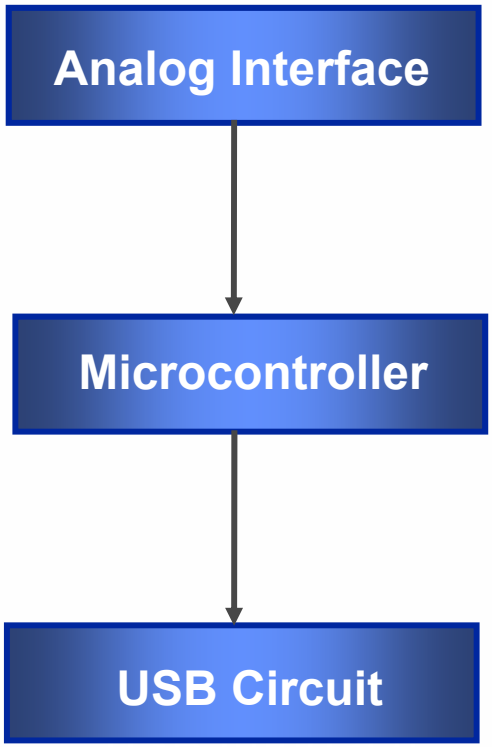


Layout Hints For 2-layer PCBs

- Start with a current return (‘ground’) plane then remove area for signal & power traces
- Place highest speed components furthest away from I/O
- Keep trace impedance and loop areas down by avoiding through-hole components whenever possible
- Use surface mount discrete components and SOIC devices if possible
- Avoid the use of vias in high threat traces (i.e. route on one layer)
- Do not share buffers in one package between high threat signals and I/Os. Always isolate them.
- Avoid unnecessary removal of return plane area around I/O connectors

PCB Design for EMC

Demo-Time!! An analog circuit!



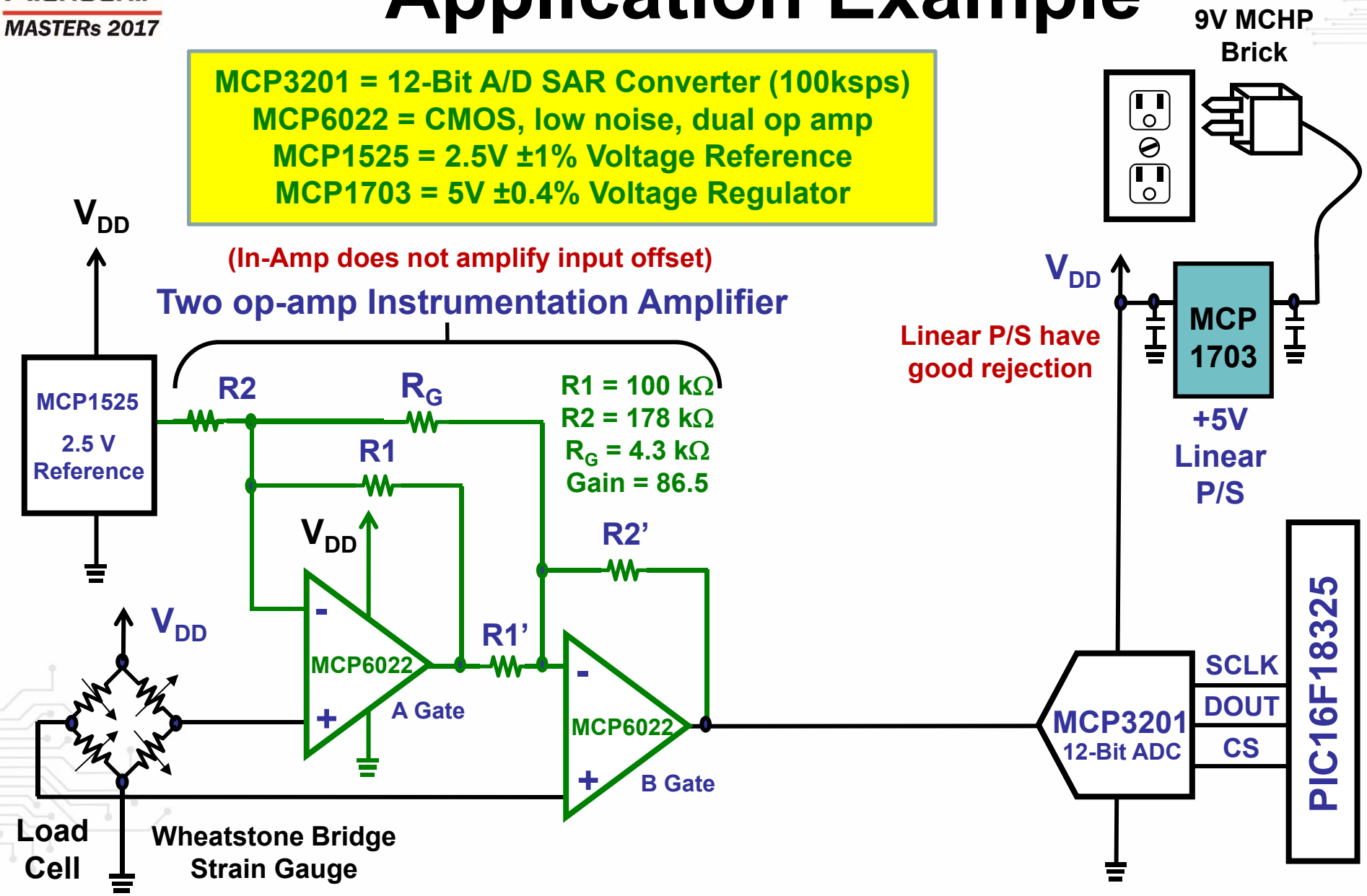
External 12-Bit ADC connected to a very stable strain gauge load cell.

The MCU controls handles the converted ADC data and sends to PC through USB.

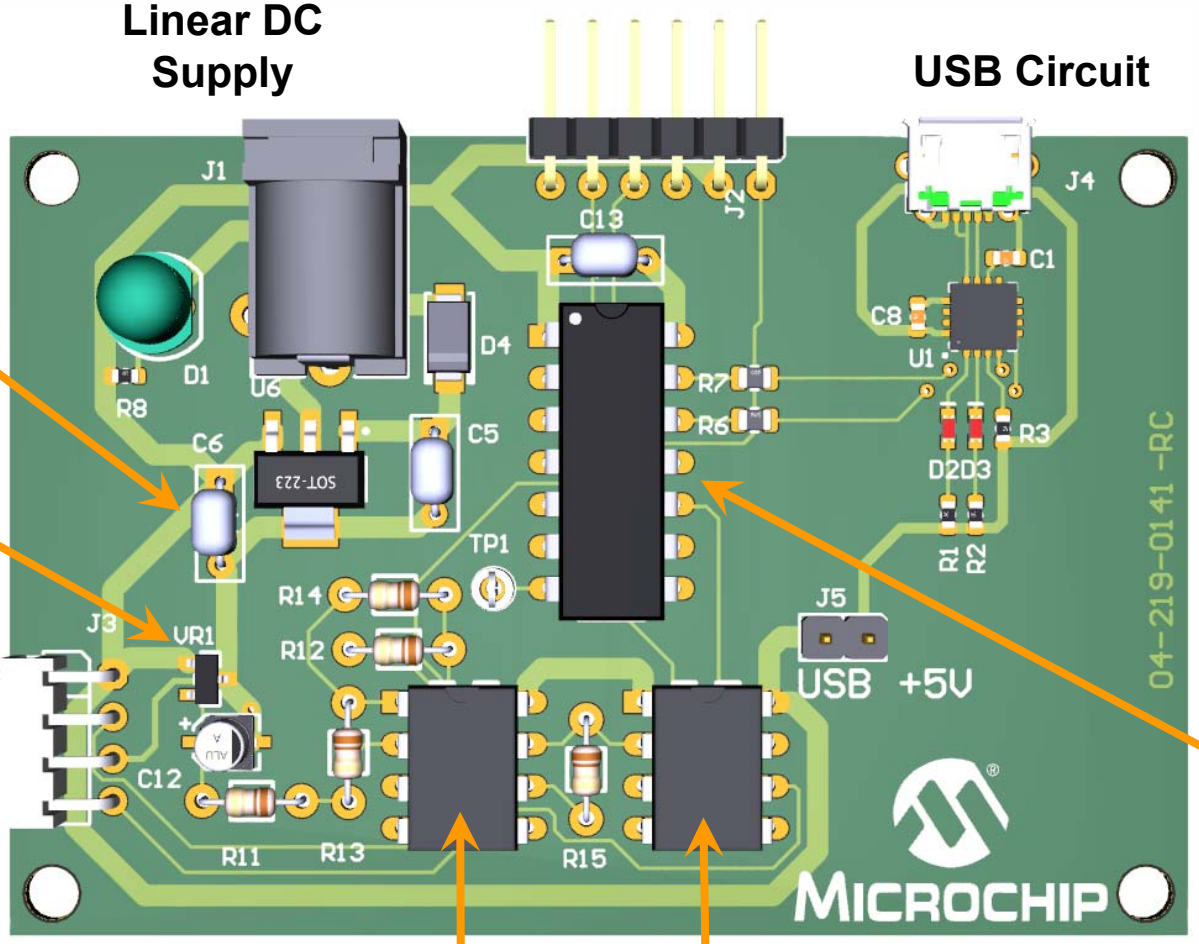
The converted ADC value is sent to PC & displayed on a histogram.

Application Example

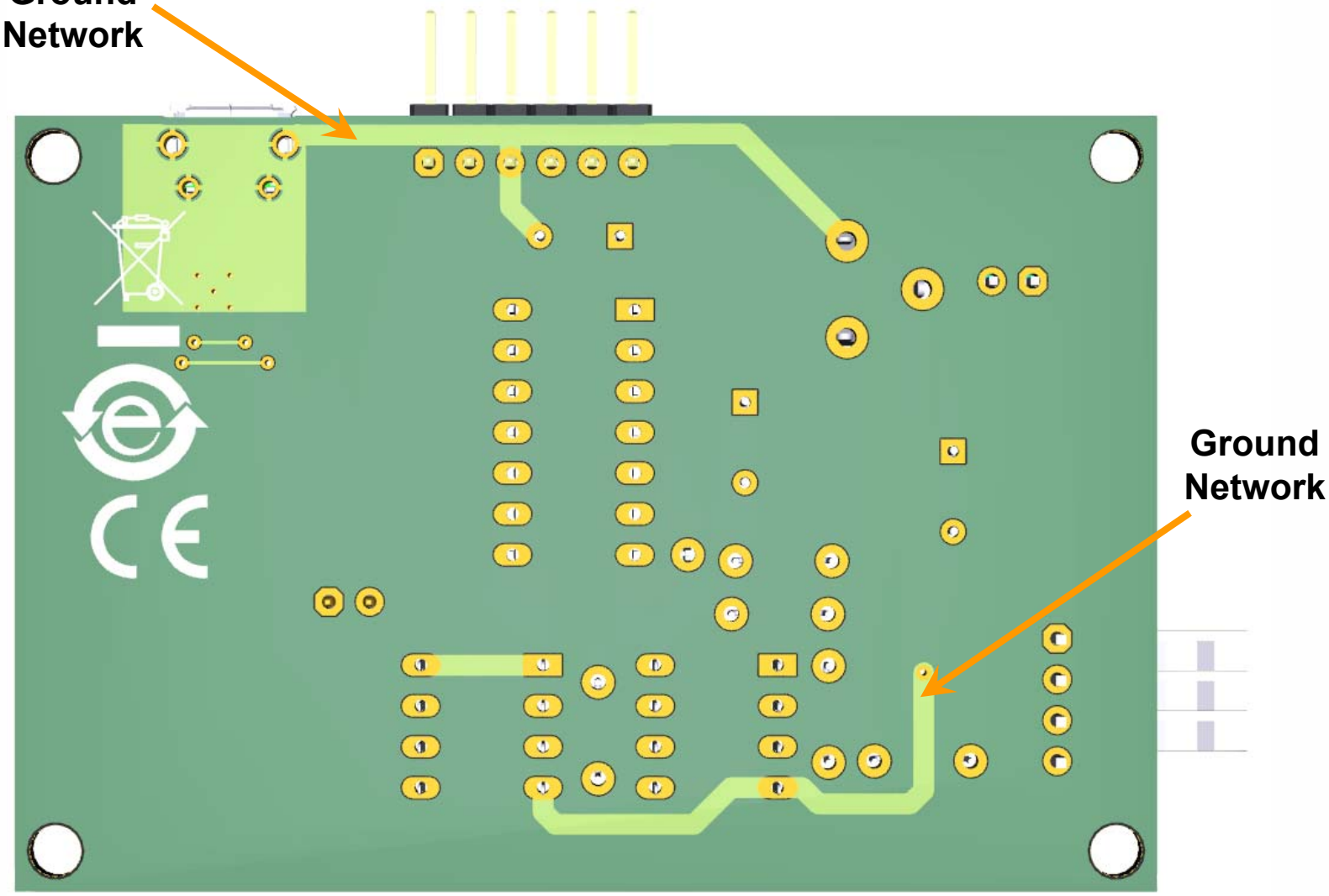
MCP3201 = 12-Bit A/D SAR Converter (100ksps)
MCP6022 = CMOS, low noise, dual op amp
MCP1525 = 2.5V ±1% Voltage Reference
MCP1703 = 5V ±0.4% Voltage Regulator



Application Board #1 (top side)



Application Board #1 (bottom side)

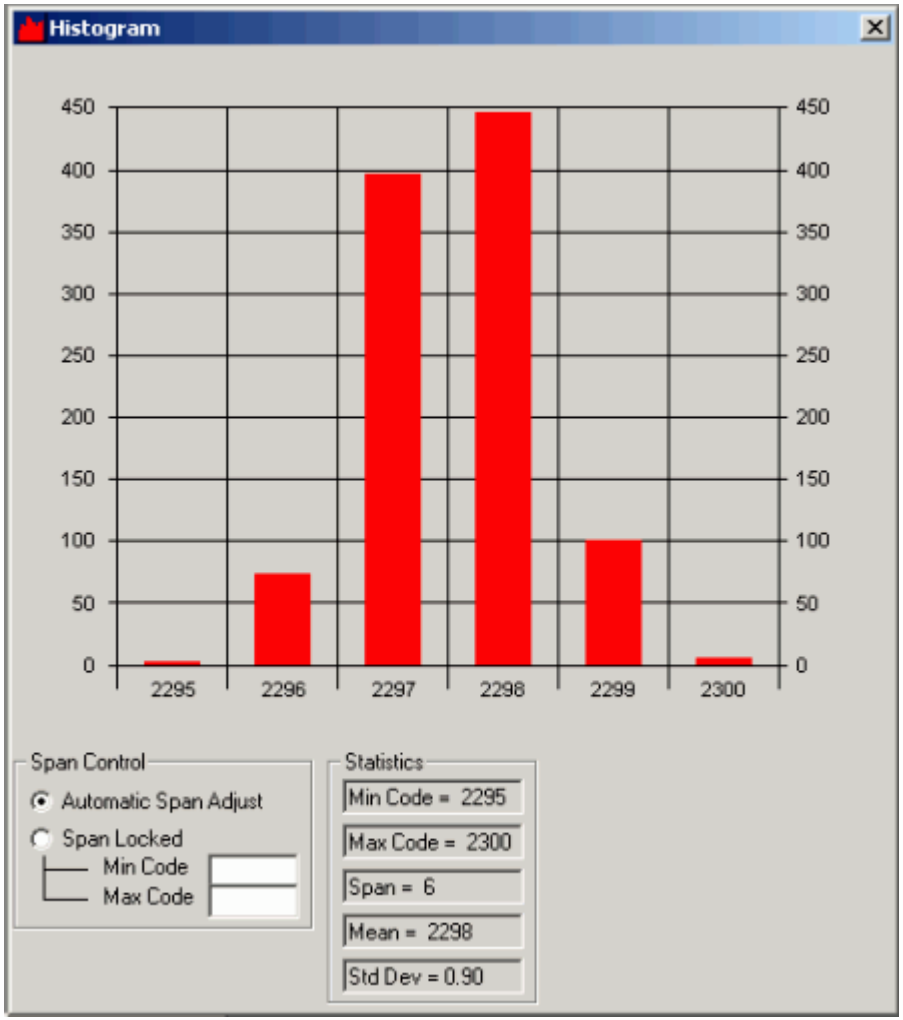


App Board #1 Test Results

Code Width of Noise = 6

(Total samples = 1024)

- **Is this good enough?**
- **Could you write an averaging routine and be okay with the results?**
- **What if the application required more accuracy?**



Noise Sources and Solutions

Power and Return Paths

Source: 50 Hz or 60 Hz line noise

Solution: Use more and better suited bypass capacitors

Source: Impedance and path loops issues

Solution: Reference plane

Noise Sources and Solutions

- **Signal Paths**

  Source: Digital switching noise USB & MCU

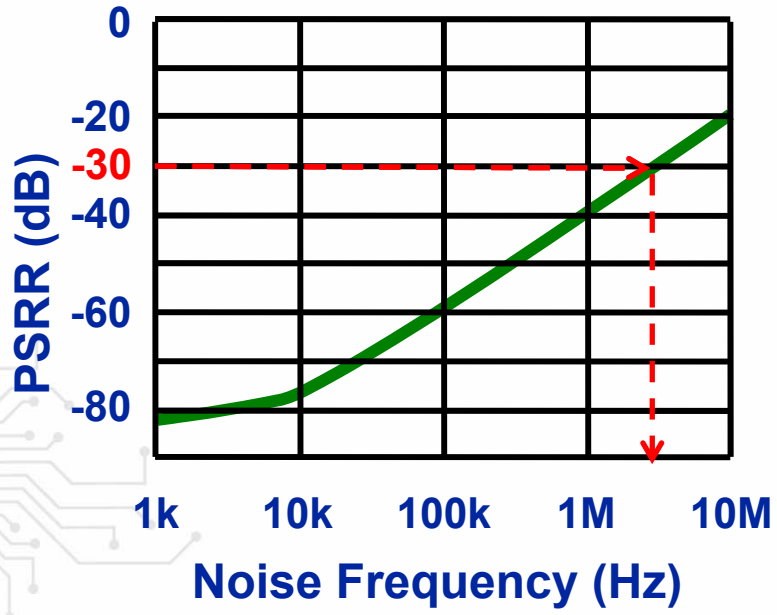
  Source: Noise generated by previous devices in chain

  Solution: Low-pass filter to ADC

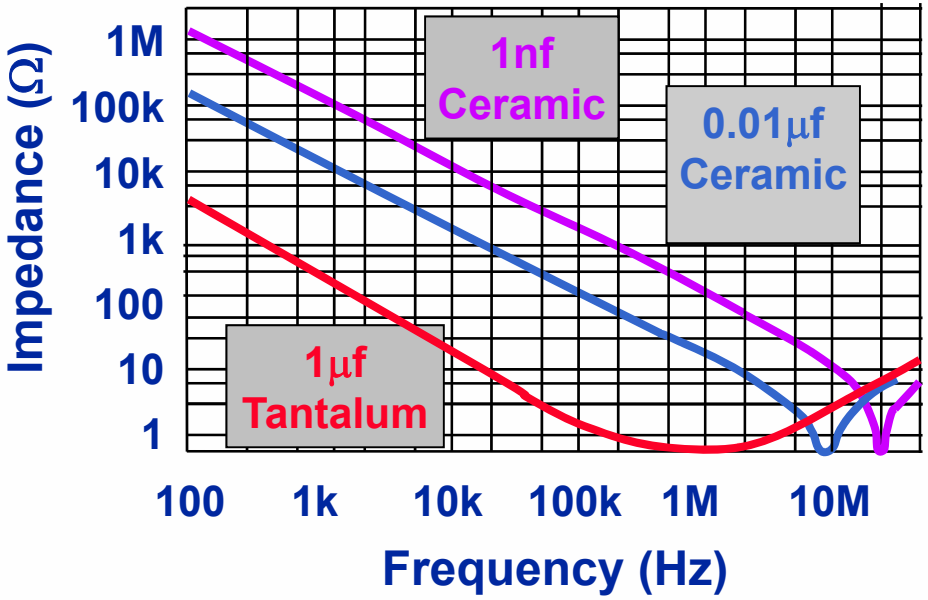
Bypass Capacitor Selection: A/D Converter Example

- **Objective:** Bring the noise to within ± 1/4 LSB (0.61 mV)
- **Assume:** Power supply = 5 V ± 20 mV (all white noise)
  - PSRR = 20 $\log_{10}(\Delta Signal/\Delta Vdd)$ = – 30.3 dB
  - Design bypass network to filter > 1 MHz

12-bit A/D Converter



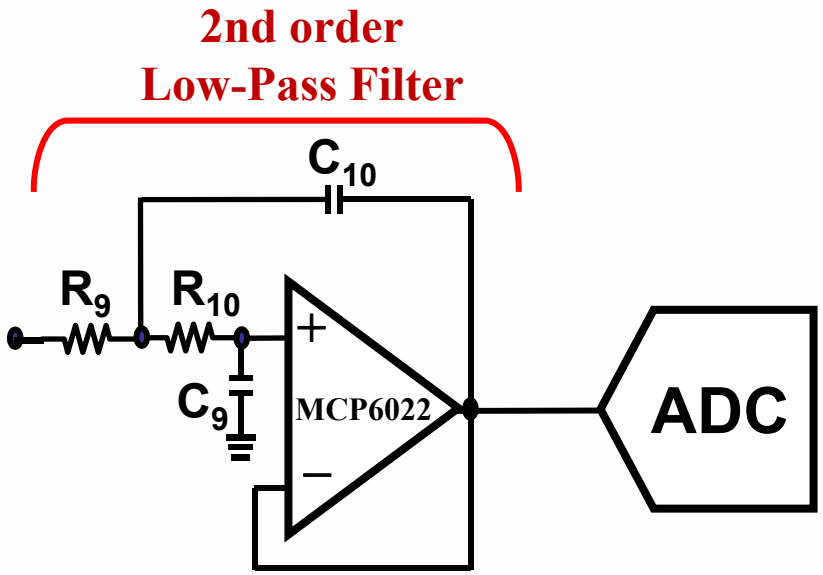
Capacitor Response



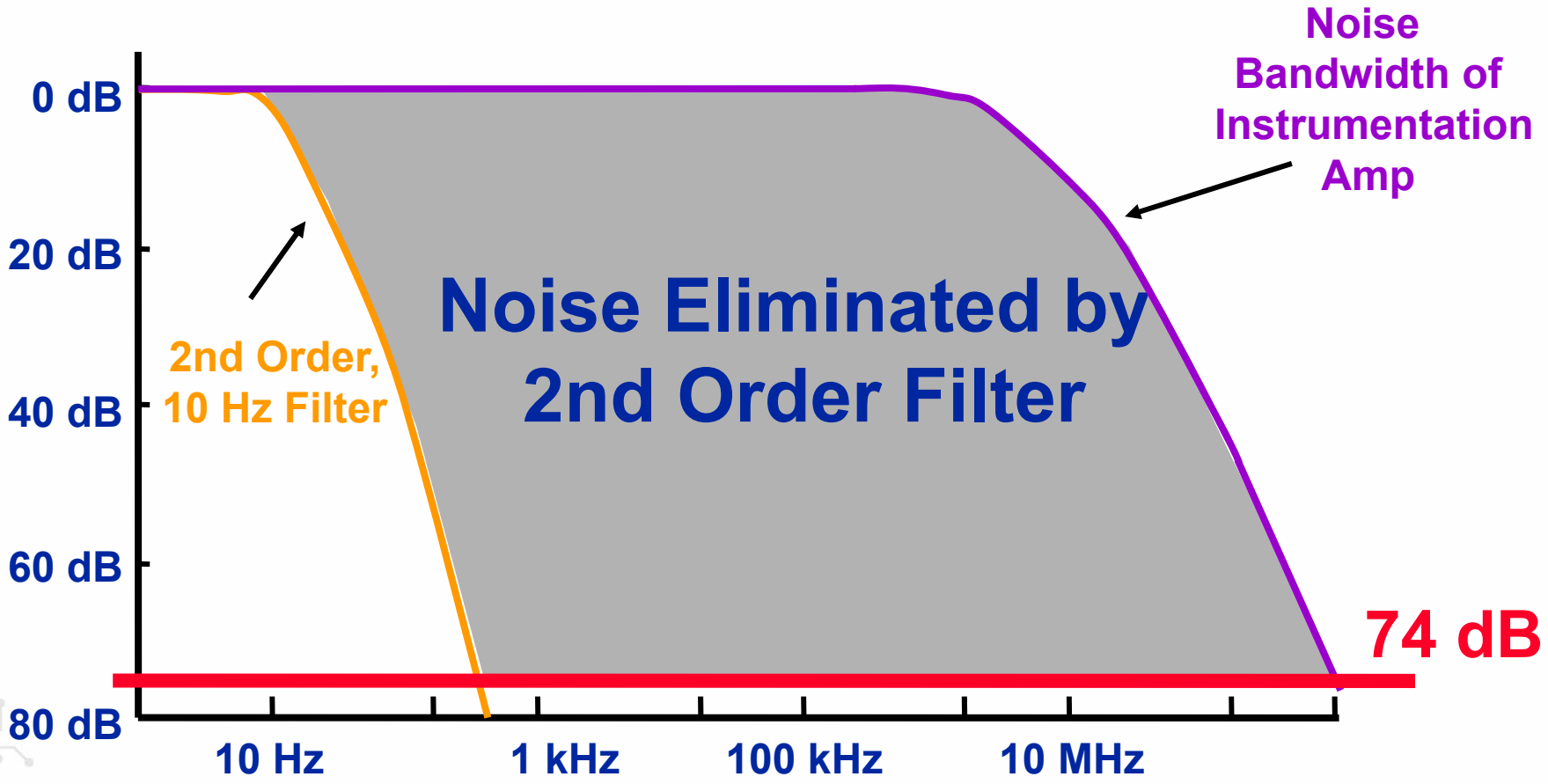
Low-Pass Filter Missing

Sallen-Key Low-Pass Filter

- Unity gain configuration
- Provides anti-aliasing filtering



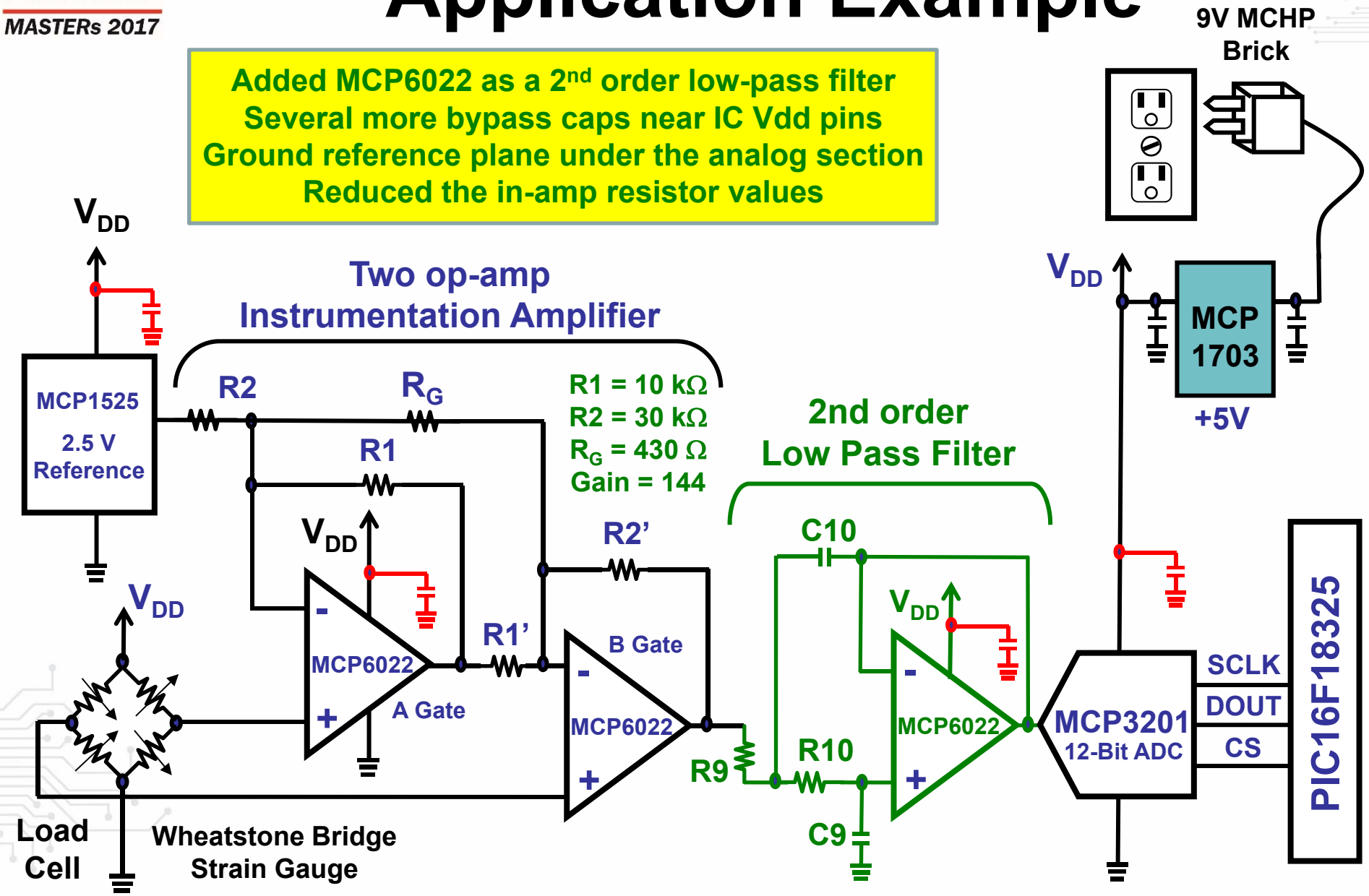
Noise Reduction with Low Pass Analog Filter



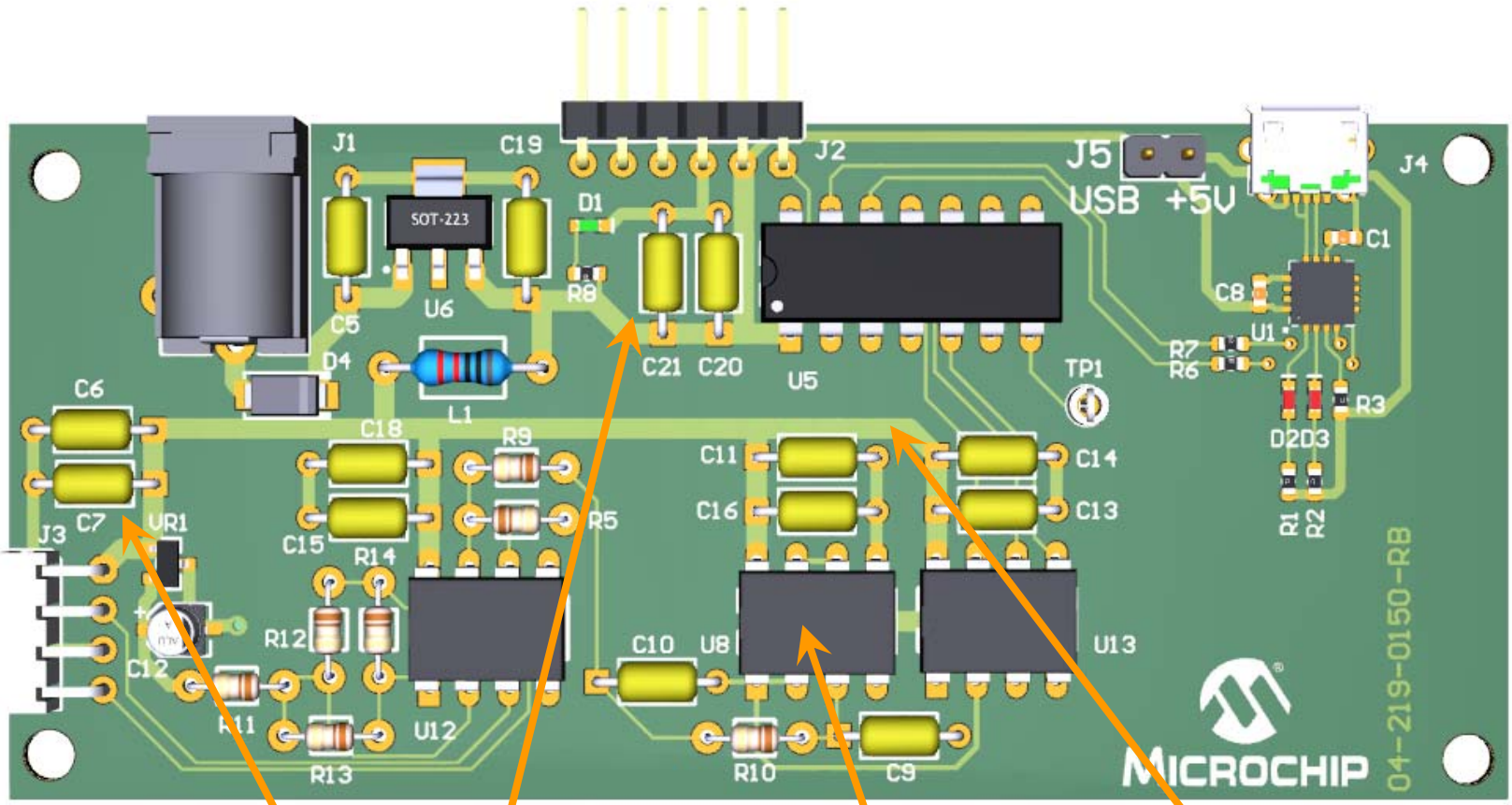
- Ideal SNR for a 12-bit A/D = (6.02 x 12) + 1.76 db = 74 dB

Application Example

Added MCP6022 as a 2nd order low-pass filter
Several more bypass caps near IC Vdd pins
Ground reference plane under the analog section
Reduced the in-amp resistor values



Application Board #2 (top side)

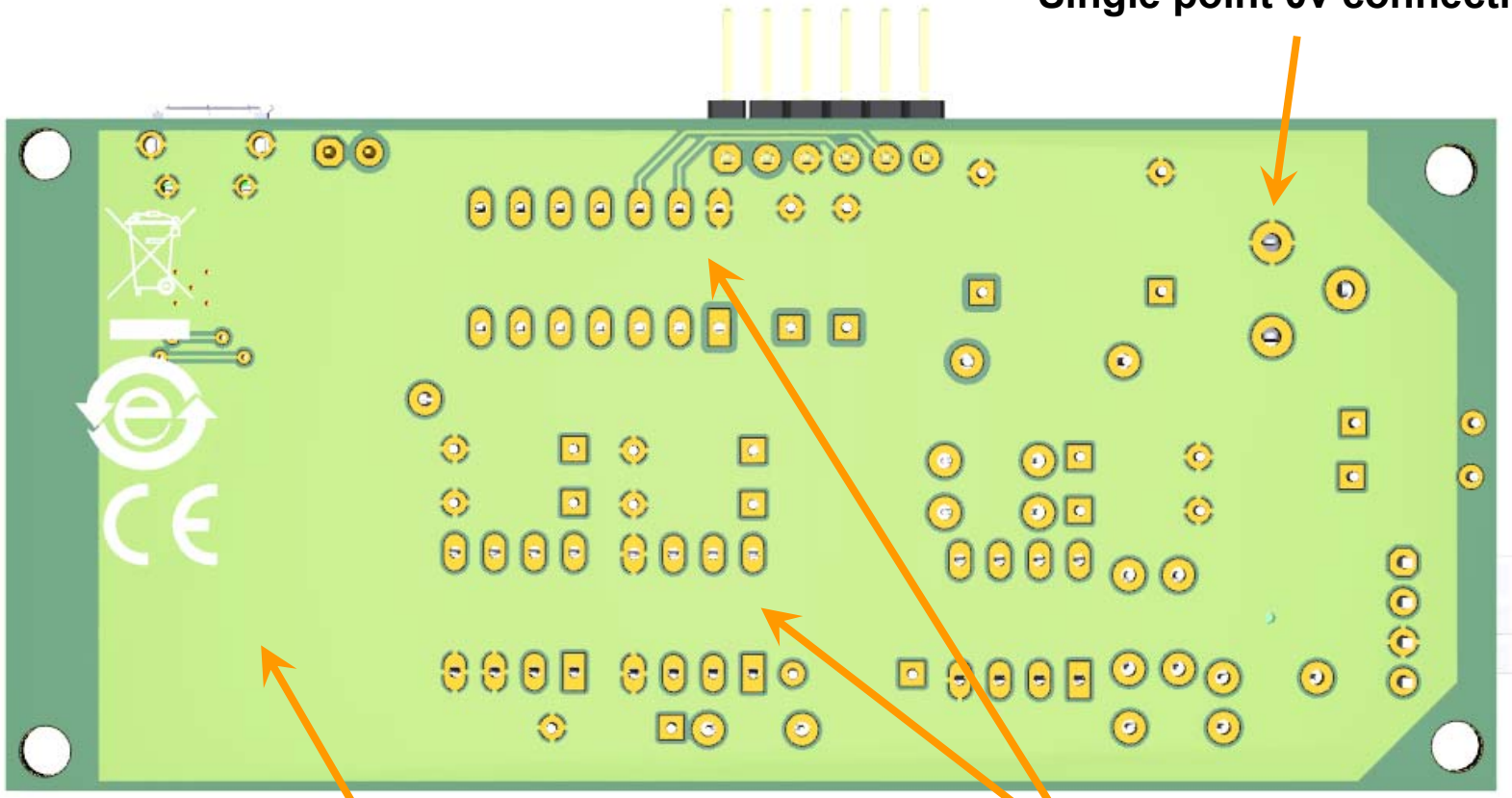


More and better suited bypass capacitors (still thru-hole)

2nd order low-pass filter

Better IC placement allows for better routing

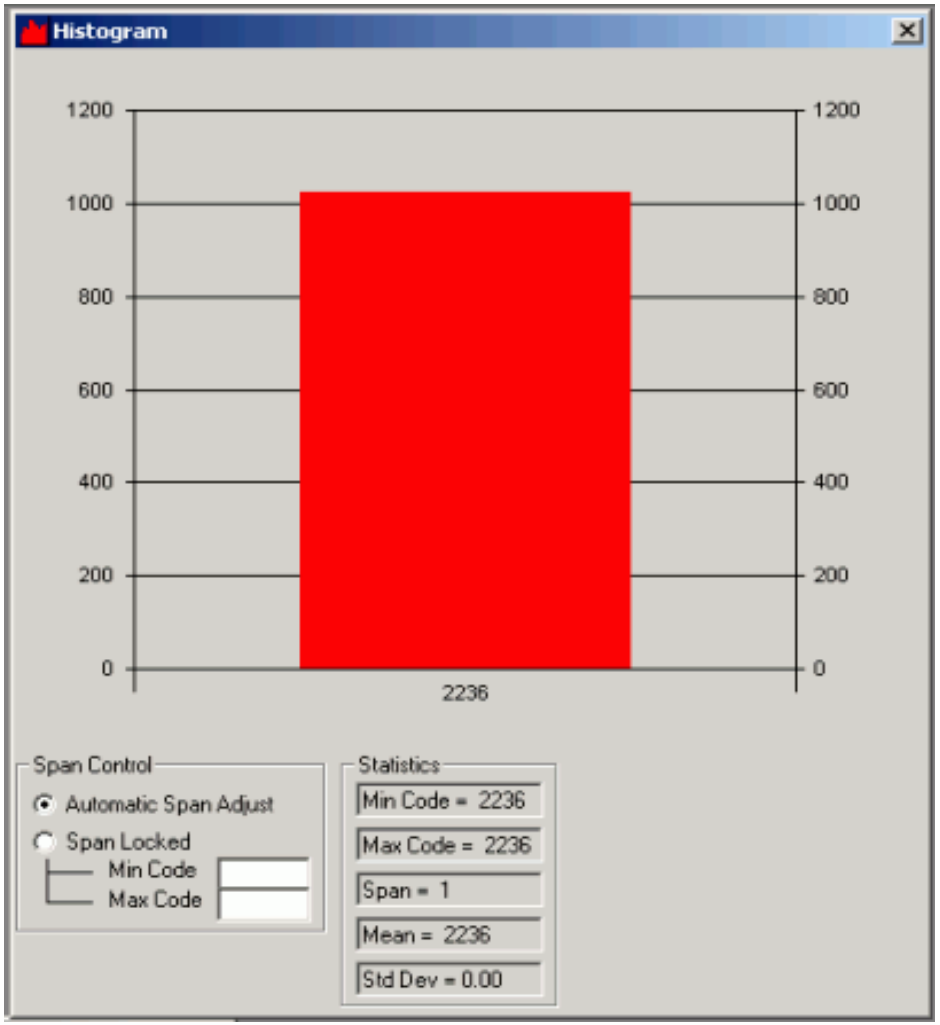
Application Board #2 (bottom side)



App Board #2 Test Results

Code Width of Noise = 1

(total samples = 1024)

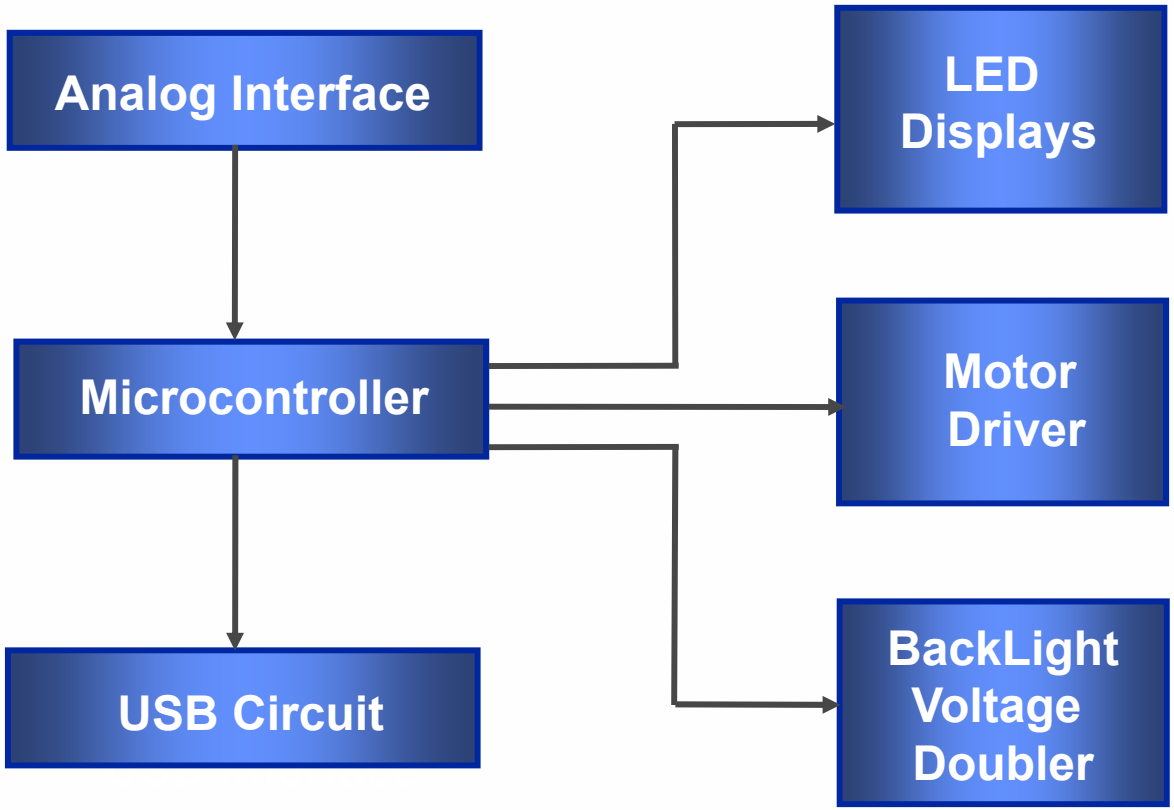


Additional Design Considerations

- Place bypass caps close to power pins
- Keep reference planes uninterrupted. Run traces around the reference planes
- Use low-noise devices
- Consider component values in order to reduce thermal noise

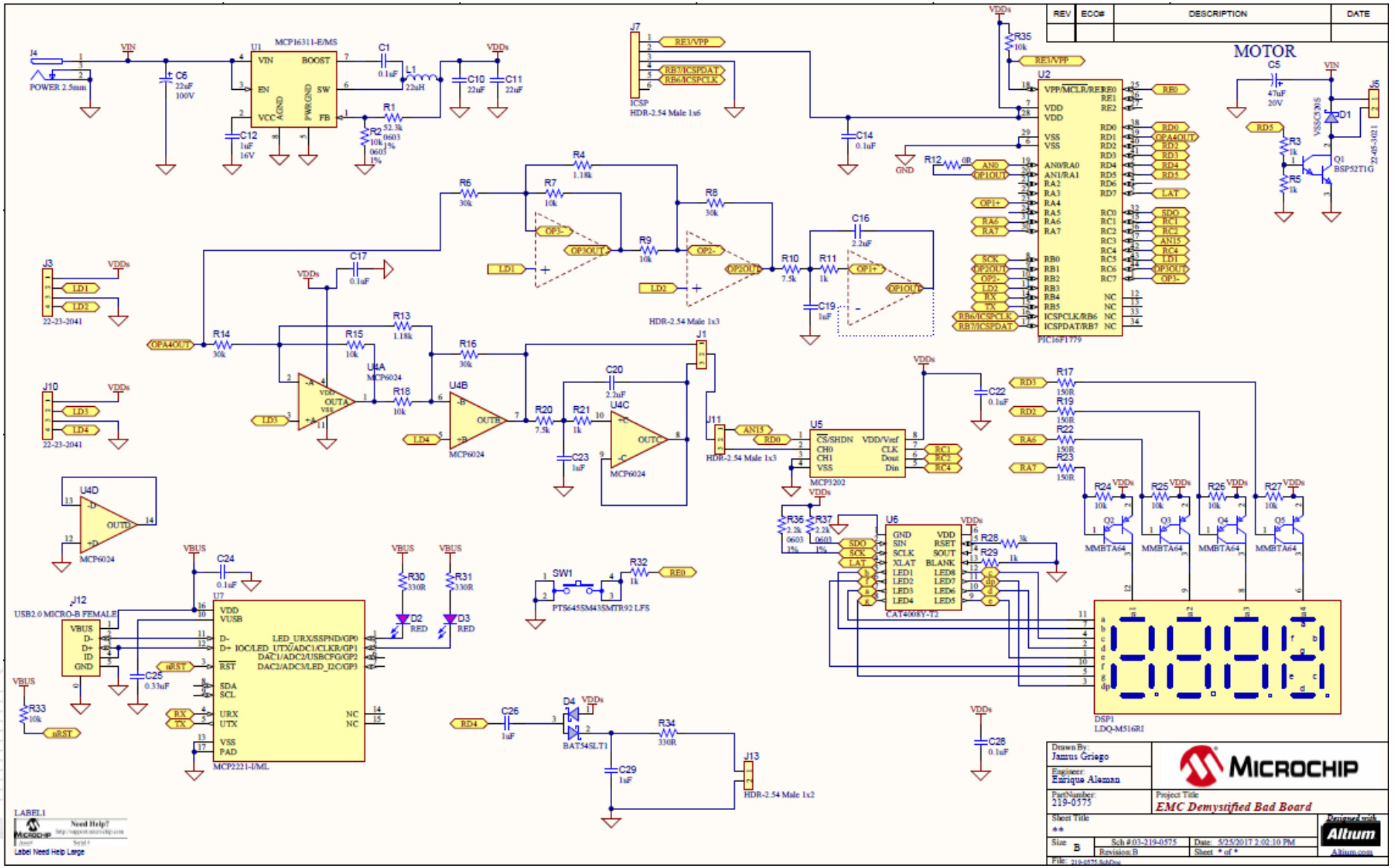
PCB Design for EMC

Demo #2: Adding some digital features!



MICROCHIP MASTERs 2017

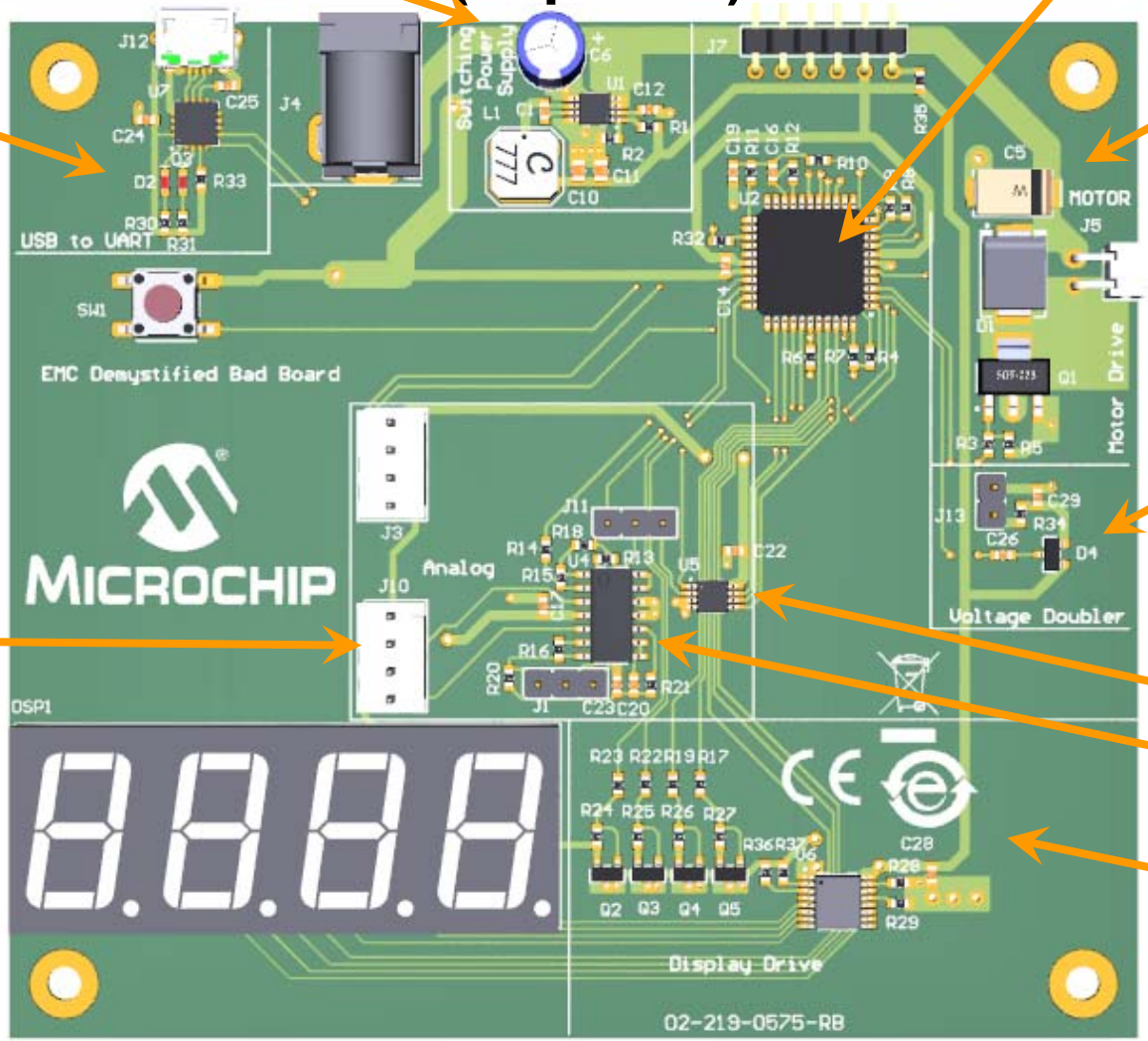
Digital Section Schematic



Design Rules of Thumb Applied

- Digital Design Rules
  - Use bypass capacitors for each IC
  - Use a diode on motor drive for back-EMF
  - DON'T modify the analog circuit
- Board Layout Rules
  - Keep bypass capacitors near IC
  - Keep supply traces short
  - Make supply traces wider
  - Avoid cuts in the reference plane

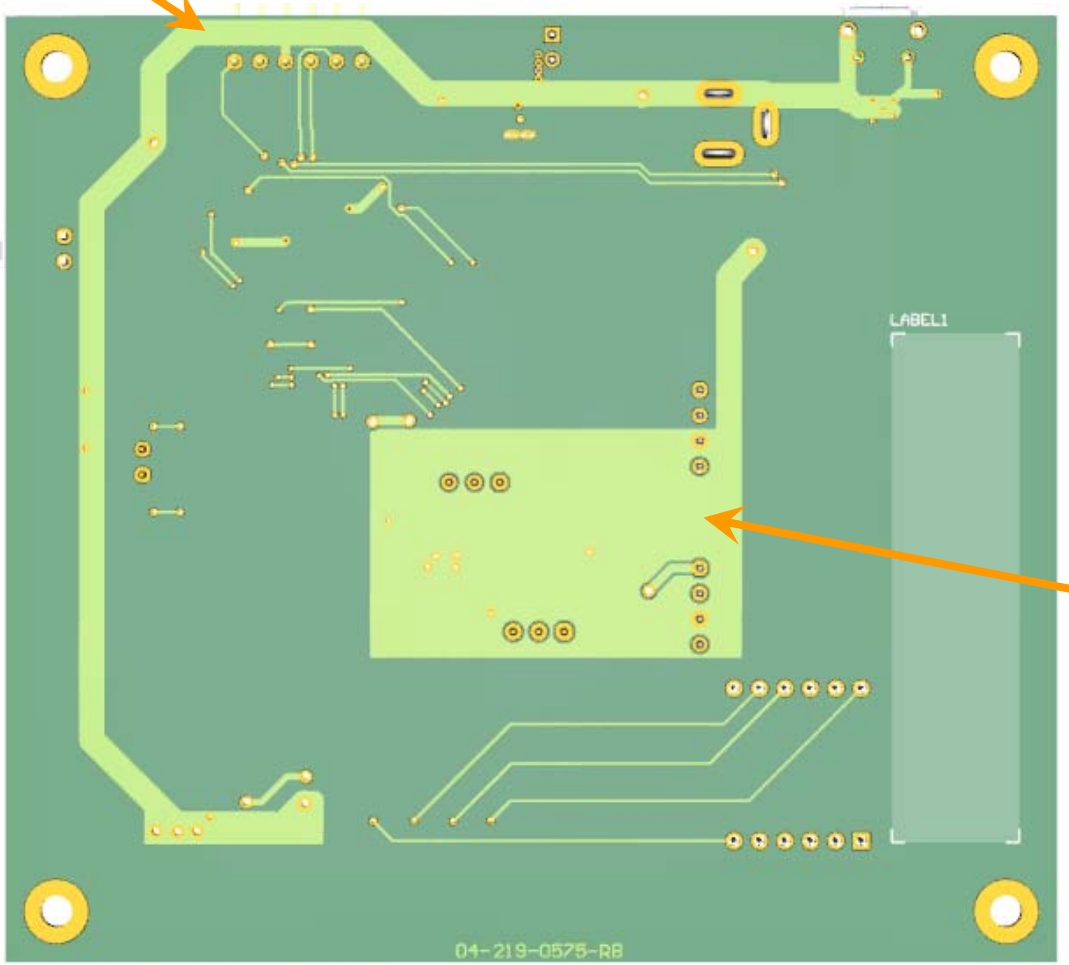
First Pass Multi-Function App Board Layout



First Pass Multi-Function App Board Layout

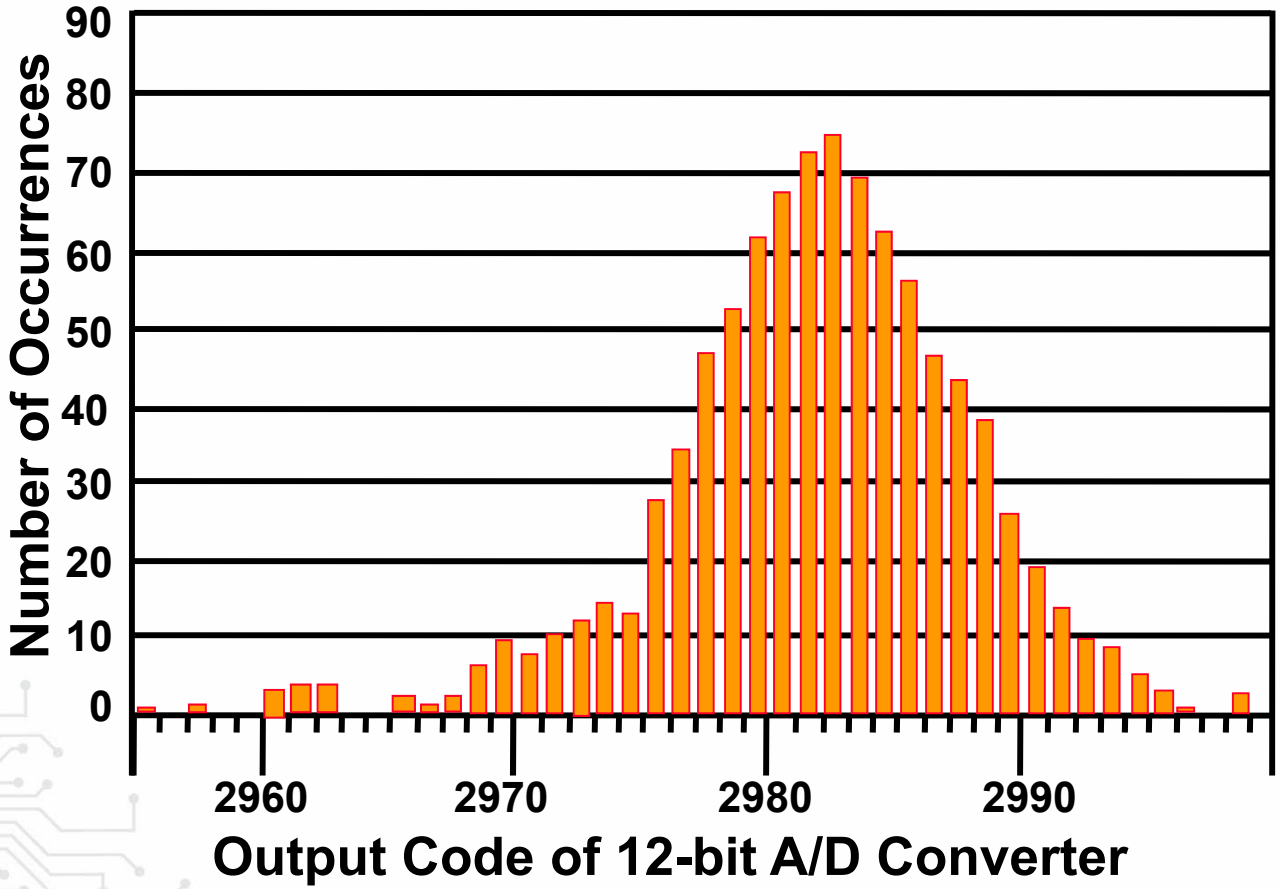
Ground Network

(bottom side)



Analog reference plane

Multi-Function App Board #3 Test Results



Code Width of Noise = 44

total samples = 1024

DENIAL!!

I didn’t touch the analog section,
IT IS NOT MY FAULT!

Second Pass on Design

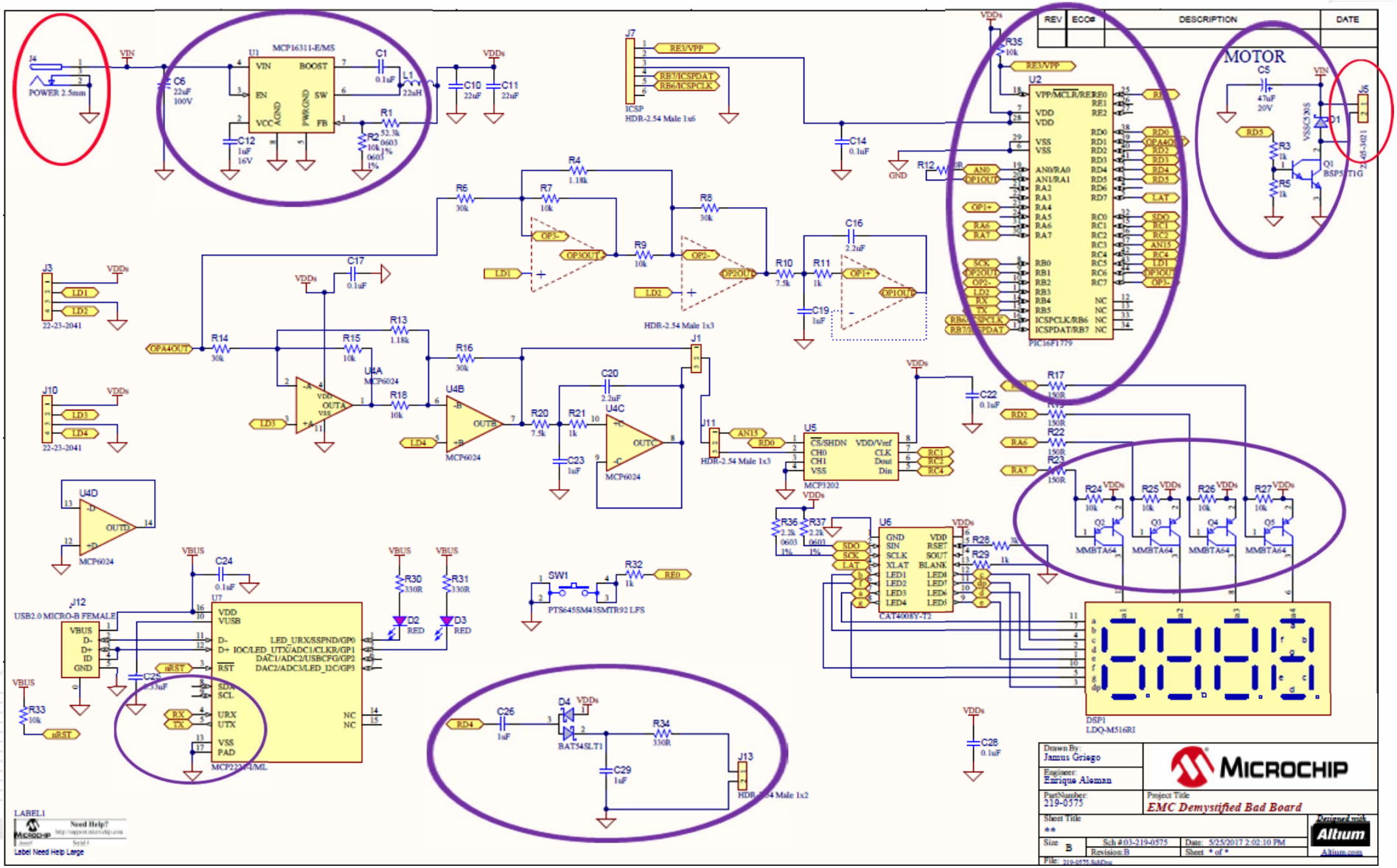
- **Apply a more systematic approach to the PCB design**
  - Identify the noise sources
  - Identify the noise pathways
  - Contain noise and minimize coupling
  - Develop a Power Distribution Network (PDN) for both the supply and the return networks

Identify the Noise Sources

- **Internal noise sources**
  - Switching noise generated by fast rise time signals
  - Switching noise generated by high voltage/current switching
- **External noise sources**
  - Externally generated Electro-Magnetic Interference or EMI
  - May be radiated or conducted into the application

MICROCHIP MASTERs 2017

Digital Section Schematic



Identifying Noise Pathways

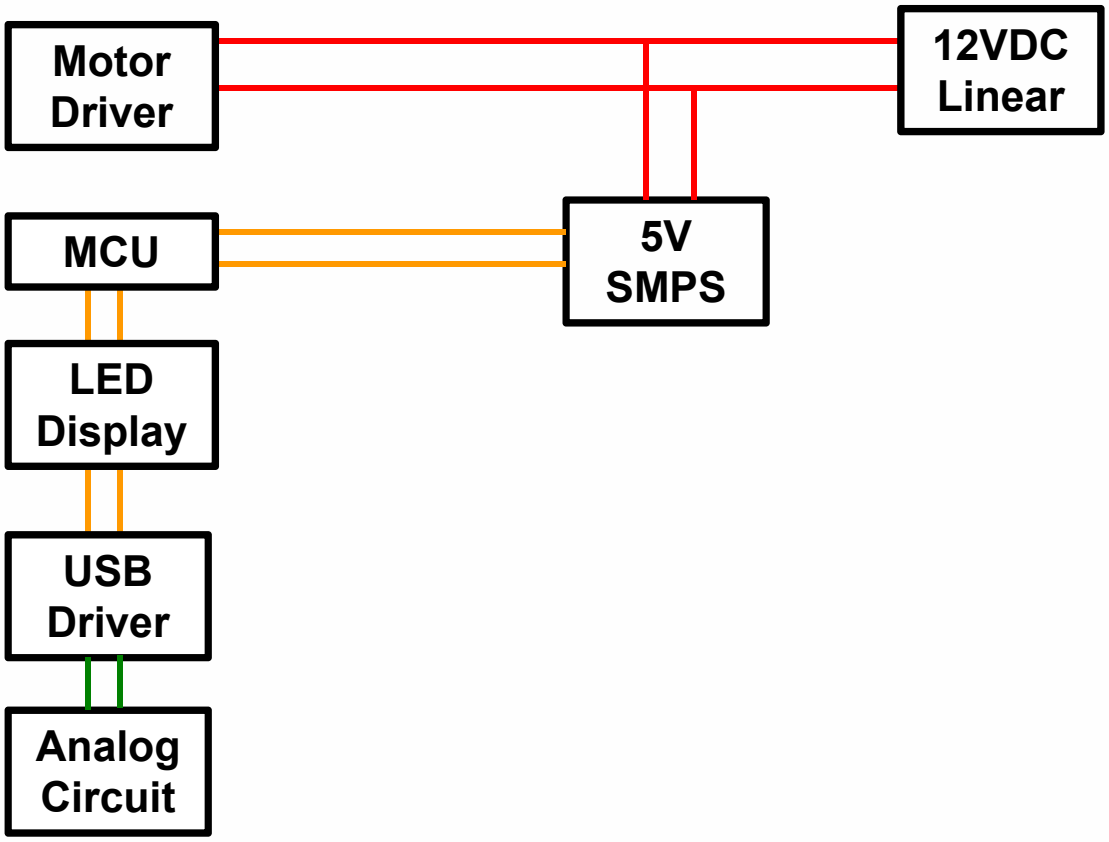
- **Pathways for Conducted Noise**
  - Power and Return currents interacting with the trace resistance and inductance
  - External wires can transport noise
- **Pathways for Radiated Noise**
  - Crosstalk: capacitively coupled fast rise time signals in close proximity
  - Magnetically coupled from high current signals in close proximity, or through a ferrous material
  - Traces acting as Antennas for incoming RFI

Map out a Power Distribution Network

- **Draw the sections of the design and add the connections**
  - Considers the circuit as a whole
  - Isolates the noise sources
  - Restricts the noise pathways

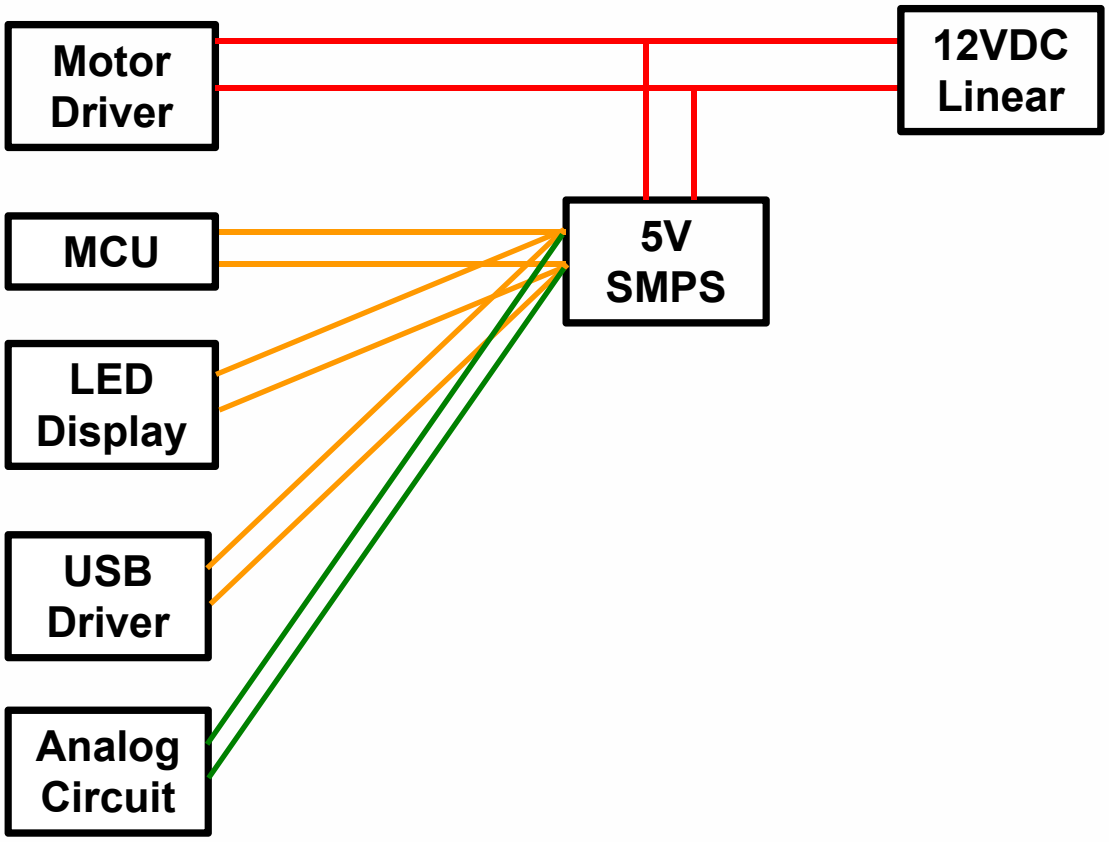
Mapping Out the Plan

- **Multipoint Plan**



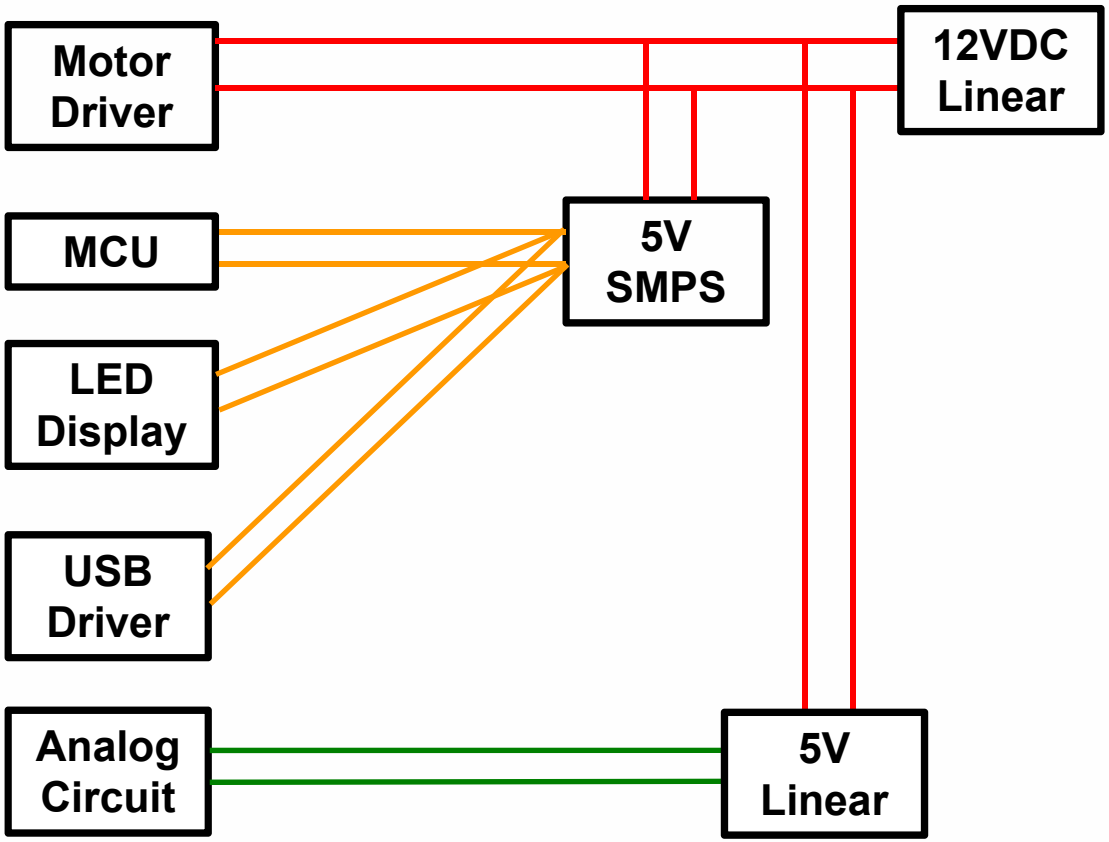
Mapping Out the Plan

- Single-Point Plan



Mapping Out the Plan

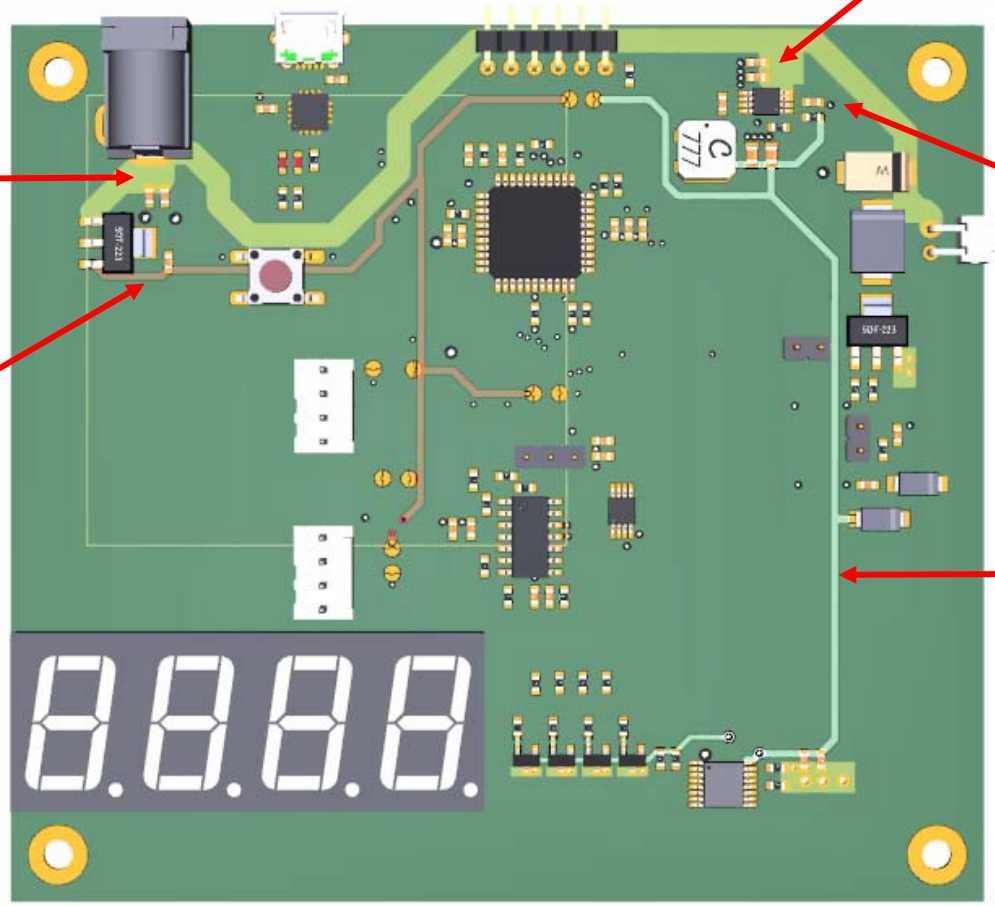
- **Modified Single-Point Plan**



Re-layout the Board

- **Layout the board using the plan**
  - Think about isolation when placing circuits
  - Think about how to route supply power and return for each section
  - Remember to isolate sensitive signals from fast-switching and high current signals
  - Remember which traces have to be wide
  - Remember which traces have to be short

Placement of Power Distribution



Wide traces for Low-Z Power Routing

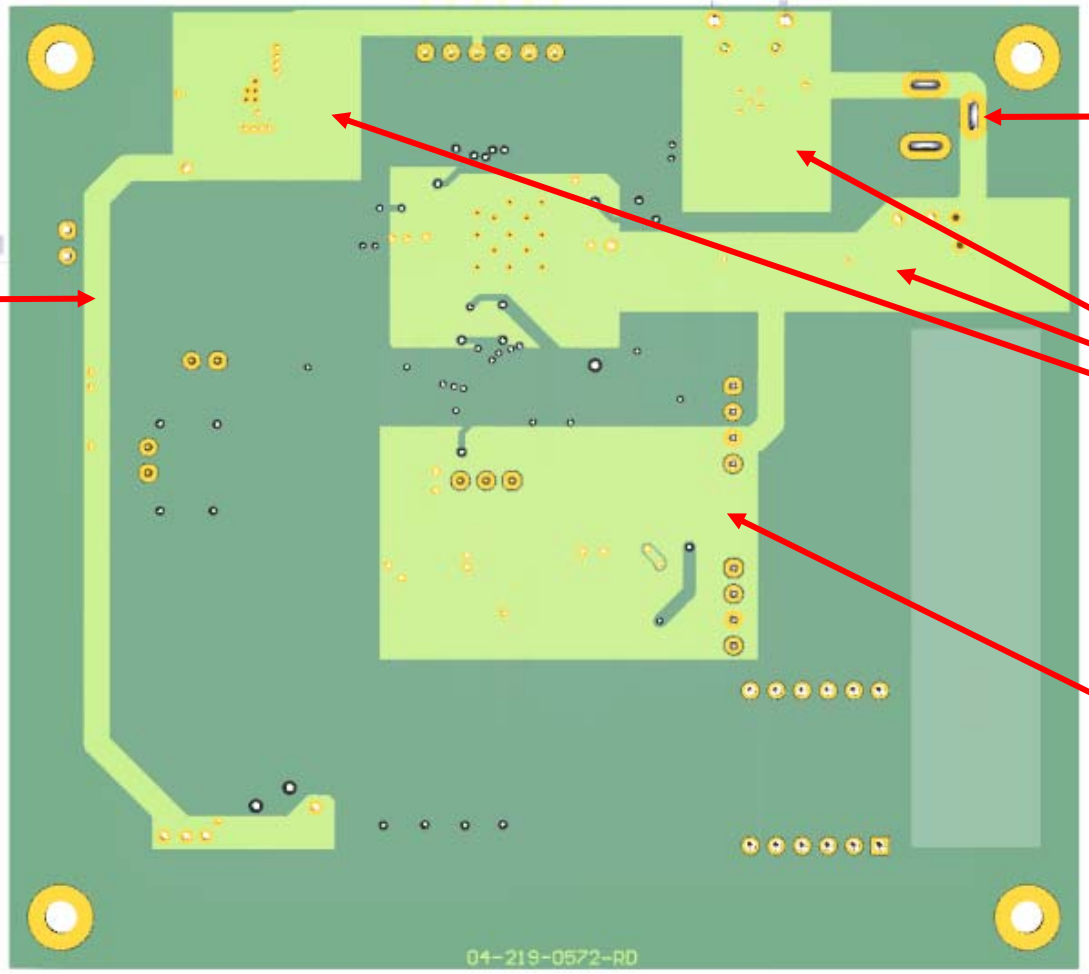
12V Supply Network

Moved SMPS to accommodate PDN

5V Linear Supply Network for Analog

5V SMPS Network for Digital

Placement of Return (GND) Distribution



Kept traces wider when they need to be routed

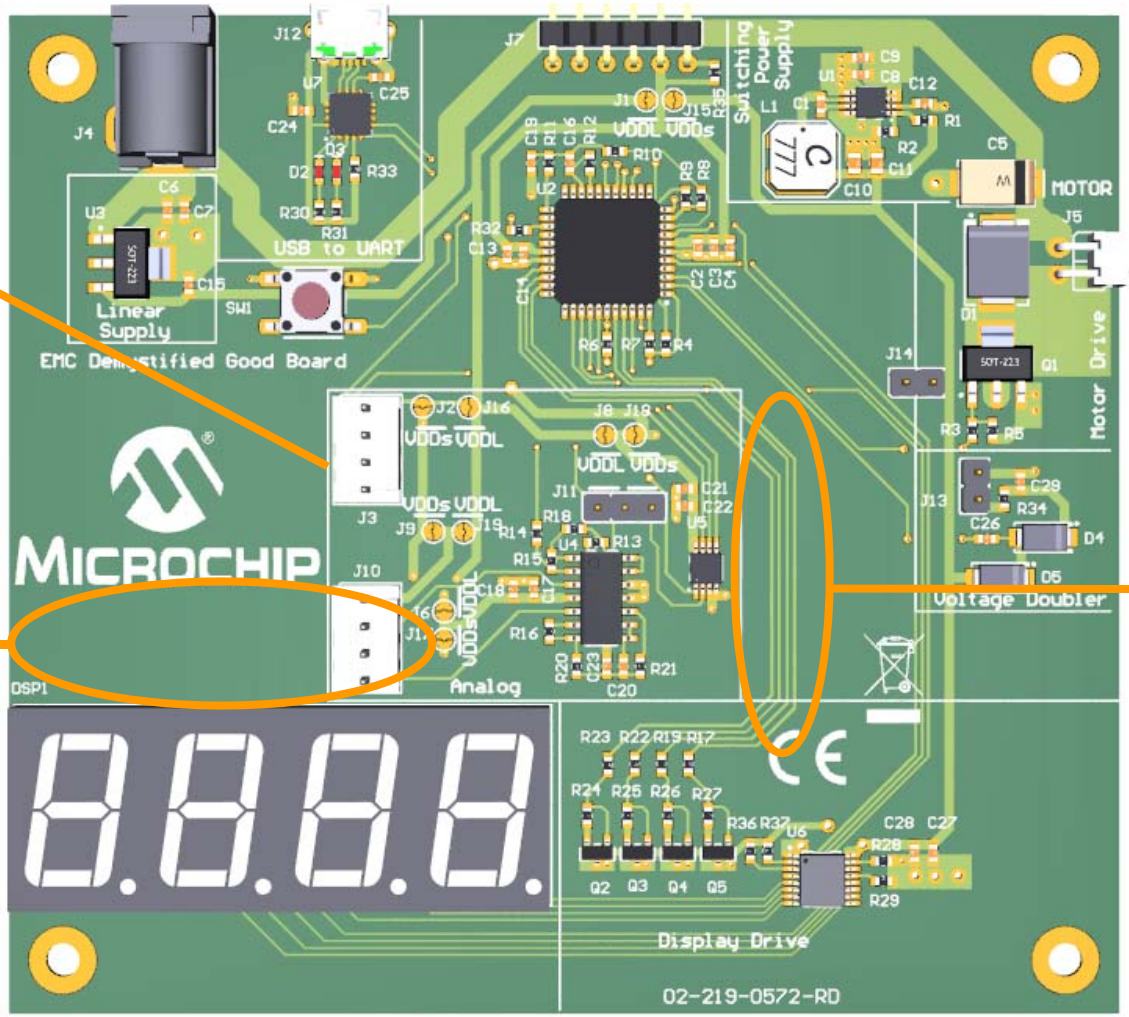
Single point return connection

Added many more reference planes

Uninterrupted analog reference plane

Application Board #4 (top side)

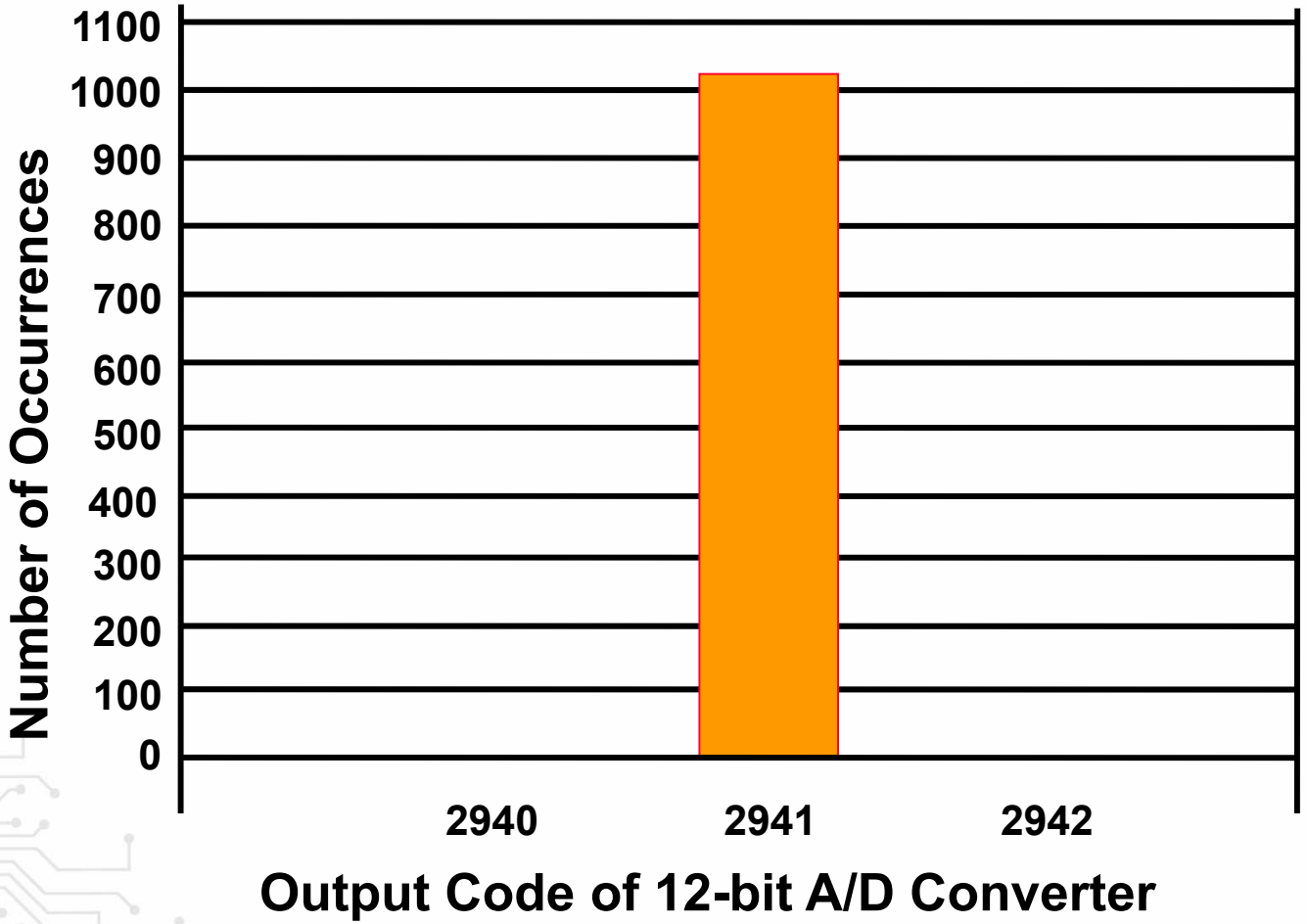
No digital signals pass through analog area



"Quiet" analog input area

Digital signals routed away from analog reference plane

Mixed Signal App Board #4 Test Results



Code Width of Noise = 1

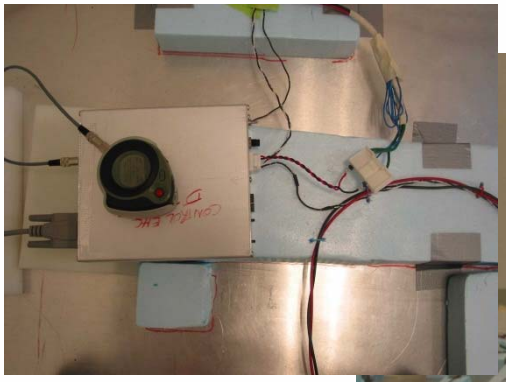
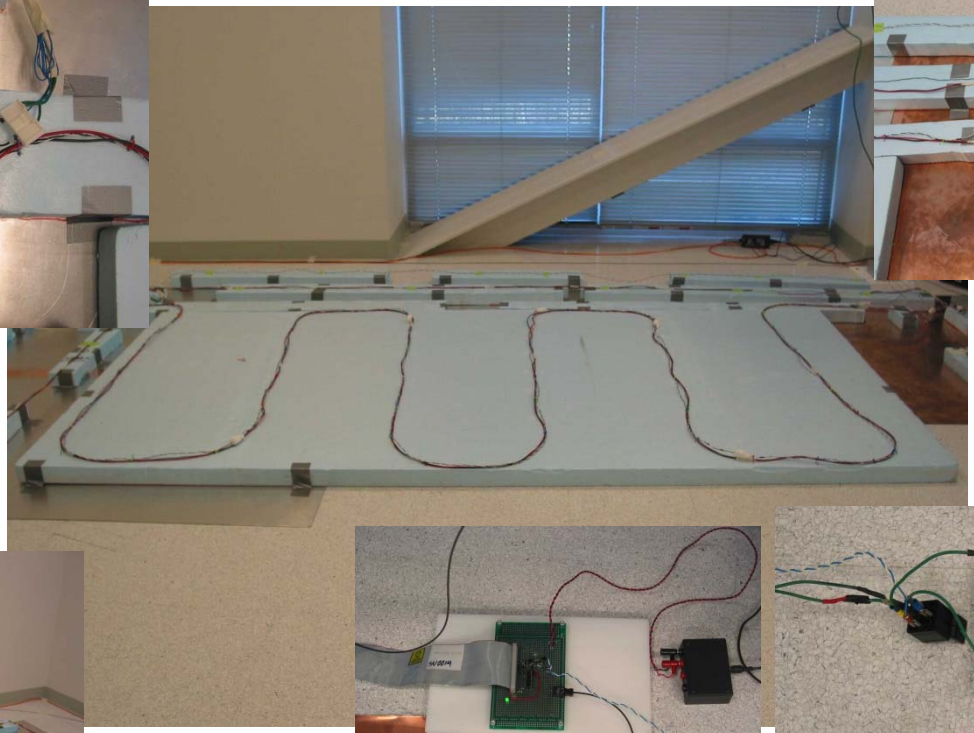
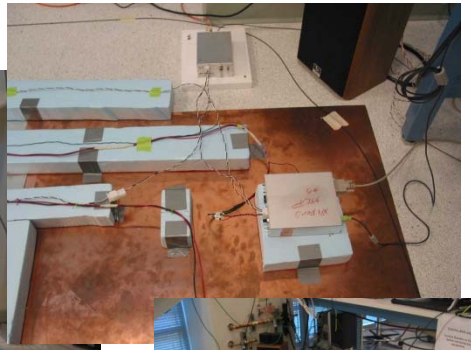
(total samples = 1024)

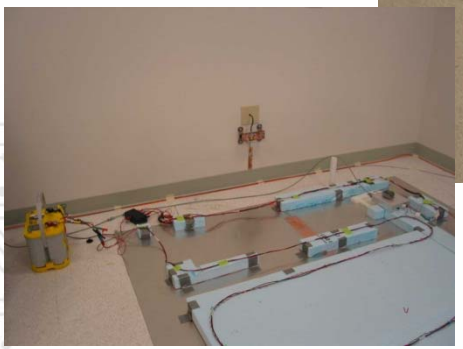
Agenda

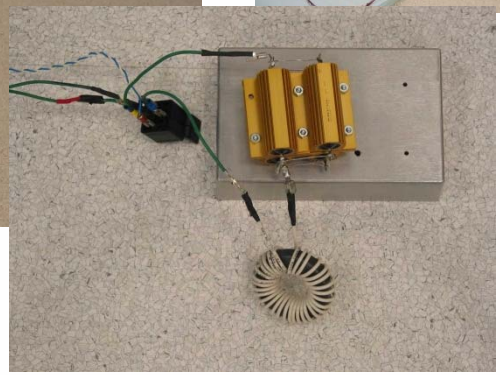
- What is ‘EMC’ and Why We Care About It
- Characteristics, Quantification and Radiation Modes of Electrical Noise
- Noise Path Control
- Signal Integrity
- Design for EMC
  - Circuit Design for EMC
  - PCB Design for EMC
- **Real-Life EMC ‘uh-ohs’!**
- EMC Guideline Summary (reference)

Power Noise Issue: Reproduce Failure

- **Simplify noise source for repeatability and ease of testing**

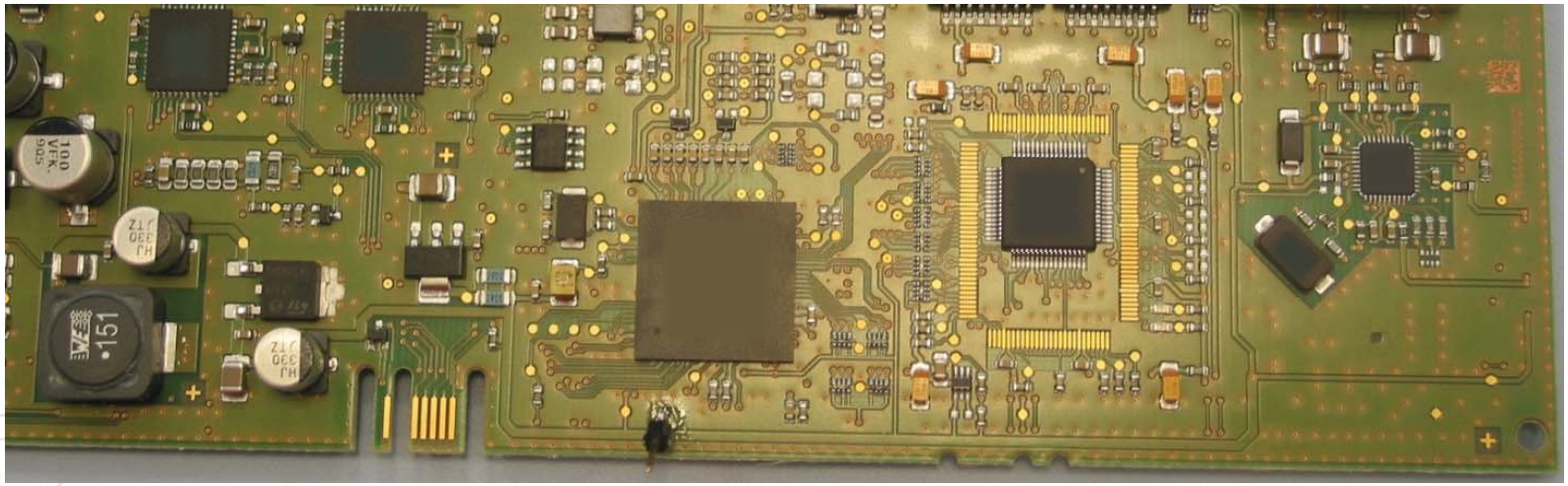




Inductor/Resistor Network

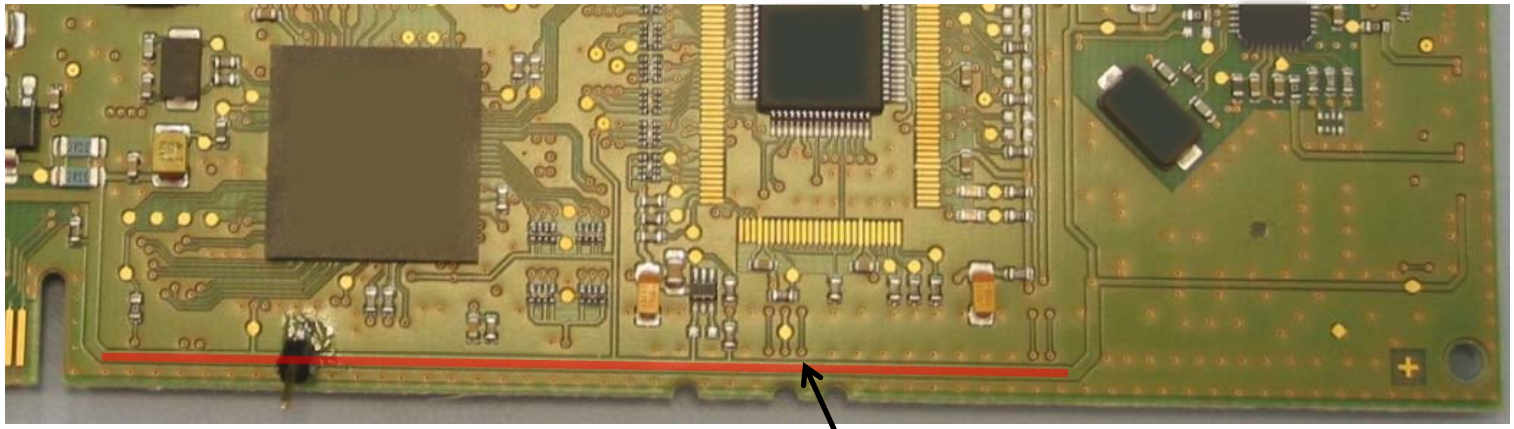
Radiated Emissions Issue: Overview

- ‘Blackbox’ module with radiated emissions failures
  - Investigate potential radiators
  - Examine power distribution network
  - Review layer stack-up



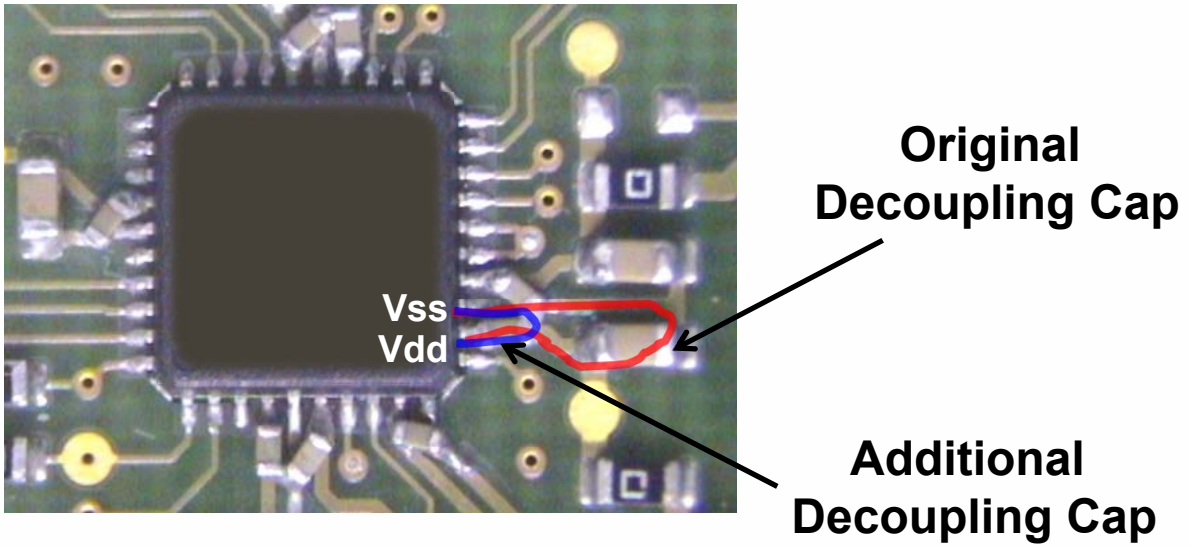
Radiated Emissions Issue: Potential Radiators

- **Trace routed near board edge**
  - Return stitching vias near board edge should reduce board edge radiation (low potential for root cause)



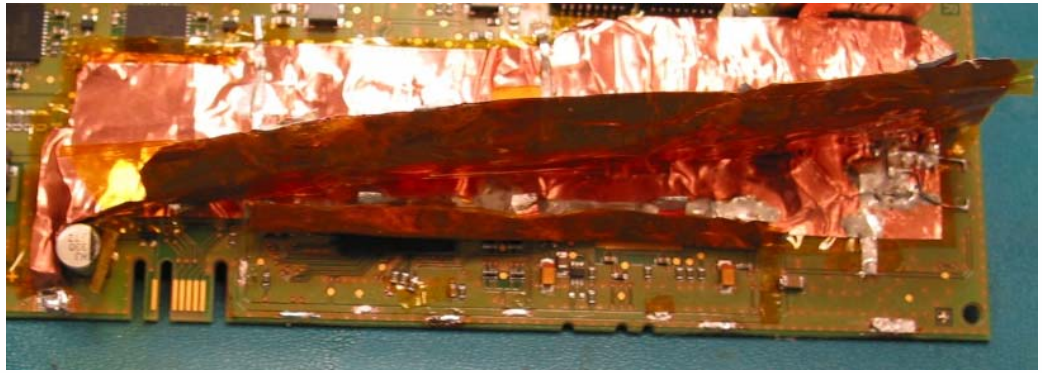
Radiated Emissions Issue: PDN

- **Poor placement of decoupling capacitors (potential root cause)**
  - Long loop path (red) – higher inductance
- **Added closer lower value decoupling**
  - Shorter loop path (blue) – lower inductance

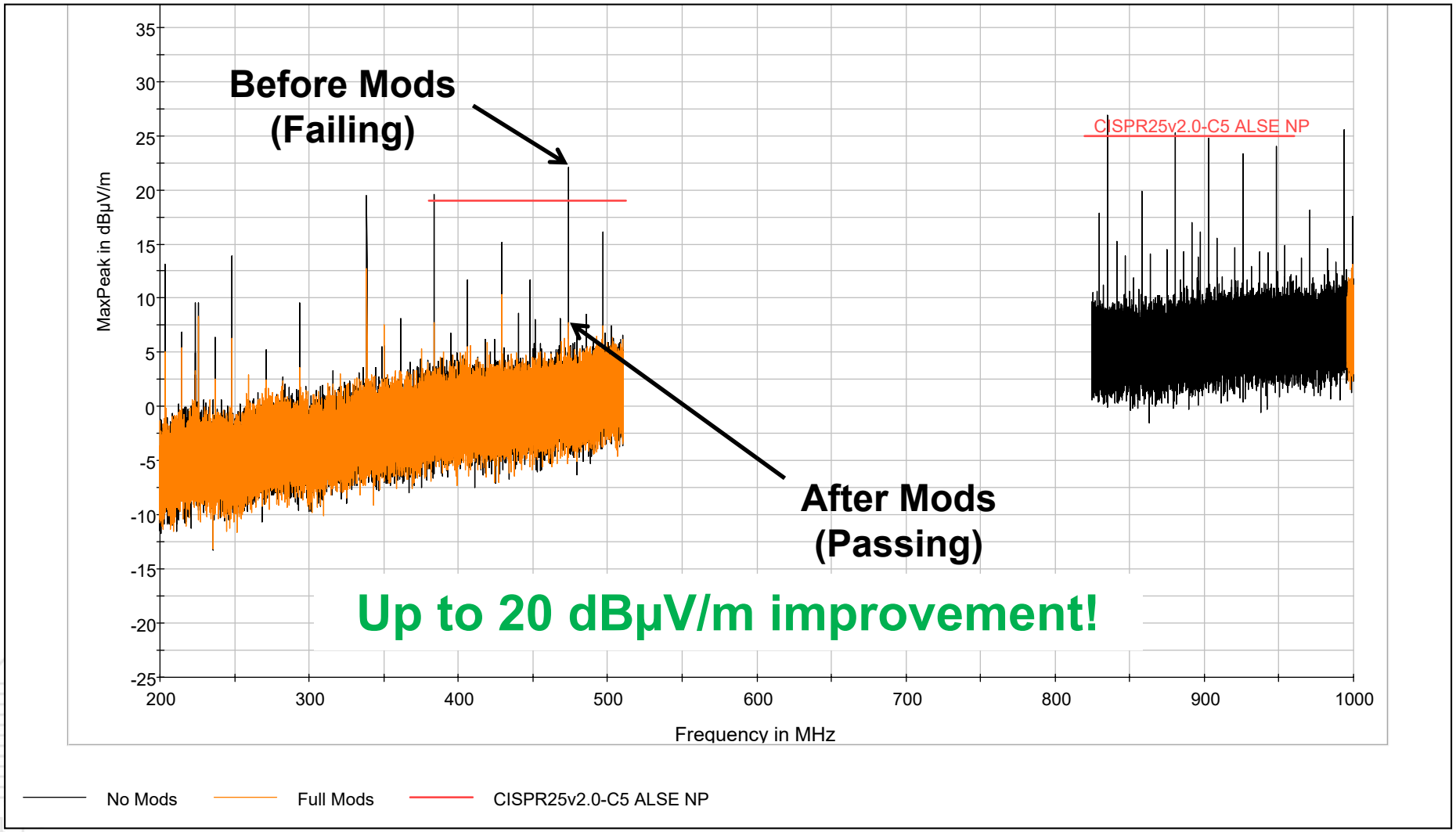


Radiated Emissions Issue: Layer Stack-Up

- **Four layer board (3 signal, 1 ground) (potential root cause)**
  - No dedicated power planes (narrow traces only)
  - Return plane split to accommodate signal routing
- **Added power/ground planes (copper tape)**
  - Lowered PDN impedance
  - Shielded potential radiators



Radiated Emissions Issue: Results



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- **EMC Guideline Summary (reference material)**

EMC Guidelines

- **Use following guidelines to assist debug of common EMC problems.**
- **Includes:**
  - Determining whether issue is radiated or conducted
  - Common application noise victims and sources
  - Application problem checklists
  - EMC and SI reference materials

Radiated or Conducted?

- **Most likely a combination of both but:**
  - Likely to be predominately conducted if problem frequencies < 30 MHz
  - Likely to be predominately radiated from cables/traces if problem frequencies between 30 MHz and 300 MHz
  - Likely to be predominately radiated from seams and cables if problem frequencies > 300 MHz

Application Noise Victims

- **Power supplies**
  - Primary noise path into more sensitive areas for conducted EFT susceptibility problems
- **Oscillator**
  - Can be highly susceptible. Spikes generate bad (timing violation) clocks within VLSI device
- **Reset**
  - Noise generates false or invalid (timing violation) resets
- **Interrupts**
  - False (or ghost) interrupts can cause problems in some RT systems. Good S/W should be able to cope though
- **Analog inputs**
  - Inherently susceptible to noise. Usually transient errors which good S/W should be able to filter. In some cases, DC rectification can generate severe offsets, resulting in operational problems

Application Noise Sources

- **Power supply loop**
  - Big radiator if decoupling cap loop not small
- **Oscillator**
  - Oscillator loop can radiate but often the phase shift caps current return loop is the worst offender if not constrained
- **Clocks**
  - Main “source of all RF evil” in most systems! Clocks MUST be as direct as possible with an identified return path close by
- **Buses**
  - Due to their length, buses are next worst offenders. High order address usually fairly quiet. Watch out for ‘ground’ bounce (loop resonance) and clock noise coupling to (long) bus lines
- **High speed peripherals (e.g. SPI)**
  - Falls into same category as clocks, just more easily (and often) ignored!
- **Clock cross coupling**
  - Clock noise can easily couple to other signals and I/O signals

Application Problem Checklist (1)

- **Check Oscillator Layout**
  - ✓ Is oscillator component loop area small (close as possible to MCU)?
  - ✓ Is current return path to V_{SS} for osc. phase shift caps as direct as possible?
  - ✓ No signals must be allowed to pass between oscillator pins or components
  - ✓ Using OSC2 to drive another device should be avoided but if necessary, is the trace guarded?

- **Check PCB power and return routing**
  - ✓ Are all HF decoupling loops as small as possible?
  - ✓ Are the right size/type of caps being used to decouple?
  - ✓ Is the PCB power partitioned correctly to provide adequate isolation?
  - ✓ Does the application contain/drive any high threat noise sources (e.g. relays)? If so, are there any potential common-mode problems?

EMI & EMS issue **EMI issue** **EMS issue**

Application Problem Checklist (2)

- **Check RESET & INTERRUPT circuitry**
  - ✓ Are pull-ups too large (susceptible)? Are pull-ups too low (noise path)?
  - ✓ Are the pull-ups connected directly to MCU Vdd?
  - ✓ Are any filter or delay caps tied directly to MCU Vss?
  - ✓ Are reset or interrupt traces long? If necessary, are they guarded?
  - ✓ Do reset or interrupts end up at an I/O connector? If so are they correctly filtered?

EMI & EMS issue **EMI issue** **EMS issue**

Application Problem Checklist (3)

- **Check PCB/system I/O**
  - ✓ Is I/O section adequately isolated?
  - ✓ Are I/O signals adequately/correctly decoupled?
  - ✓ Do any high-speed signals pass near or through I/O connector(s)?
  - ✓ If any of the outputs are high frequency, has slew rate been limited? Is I/O connector type, pinout and connectivity such that good cable shielding is possible?
  - ✓ Could any I/O exceed MCU Vin max. spec limit? If so, is it adequately current limited and filtered?
  - ✓ Are any analog signals adequately isolated and filtered?

- **Check system grounding**
  - ✓ Are application sub-systems correctly referenced off board?
  - ✓ If shielded cable is being used, is it correctly terminated?
  - ✓ If used, is line power adequately filtered? Is filter correctly located and noise return path identified and isolated?

EMI & EMS issue **EMI issue** **EMS issue**

Common EMC Standards

- **Conducted emission**
  - IEC 61000-3-2/3, EN55022: line power disturbance
  - FCC Part 15
- **Radiated emission**
  - IEC 61000-4-3
  - CISPR-11
  - FCC Part 15
- **Conducted susceptibility**
  - IEC 61000-4-4: EFT (electrical fast transients)
  - IEC 61000-4-5: lightning
- **Further information available at:**
  - http://en.wikipedia.org/wiki/List_of_EMC_directives
  - http://www.hottconsultants.com/regulations.html
  - http://www.cvel.clemson.edu/auto/auto_emc_standards.html
  - http://www.cvel.clemson.edu/emc/tutorials/commercial_emc_standards.html

What is FCC 'Part 15'?

- **Refers to Part 15 of Title 47 of the Code of Federal Regulations (47 CFR 15)**
- **Focus on emissions (radiated and conducted)**
  - "Any intentional or unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9000 pulses (cycles) per second and uses digital techniques……."
  - Applies to any such product to be advertised or sold within the United States
- **Defines 2 classes with multiple subparts:**
  - Class A: marketed for use in commercial, industrial or business environments
  - Class B: marketed for use in residential environment, but includes use in commercial industrial or business environments

    Reference:
    https://www.fcc.gov/bureaus/oet/info/documents/bulletins/oet62/oet62rev.pdf
  - *OET Bulletin 62 "Understanding FCC Regulations for Computers and other Digital Devices"*

EMC/SI References

- **Reference Books**
  - High-Speed Digital Design: A Handbook of Black Magic, Howard Johnson and Martin Graham, Prentice Hall, 1993.
  - Noise Reduction Techniques in Electronic Systems, (2nd Ed.), Henry Ott, John Wiley, N.Y., 1998.
  - EMC at the Component and PCB Level, Martin O'Hara, Newnes, 1998.
  - EMC and the Printed Circuit Board, Mark Montrose, IEEE Press, 1998.
  - The RF Capacitor Handbook, from American Technical Ceramics Inc.
  - The Circuit Designer's Companion, by Tim Williams.
  - Reference Data for Engineers, 7th edition Edward C. Jordan, Editor in chief.
  - ABC's of Transformers & Coils,by Edward J. Bukstein.
  - Signal and Power Integrity – Simplified, by Eric Bogatin

EMC/SI References

- **Application Notes**
  - TB3013 – Using the **ESD** Parasitic Diodes on Mixed Signal Microcontrollers
  - TB3121 – Conducted and Radiated Emissions on 8-bit Mid-Range Microcontrollers
  - AN823 – Analog Design in a Digital World Using Mixed Signal Controllers
  - AN949 – Making Your Oscillator Work
  - AN1778 – Class B Safety Software Library for PIC® MCUs and dsPIC® DSCs
  - AN1779 – Class B Safety Software Library for 8-bit PIC16 MCUs
  - AN1785 – ESD and EOS, Causes, Differences and Prevention
  - AN1817 – Using a Hardware or Software CRC with enhanced core microcontrollers
  - AN1848 – 8-bit PIC MCU Safety Manual
  - DS50002178 – Compiler Functional Safety Manual

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Questions?

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