Sensor Fusion at the Edge with Spartan-7
No FPGA Experience Required

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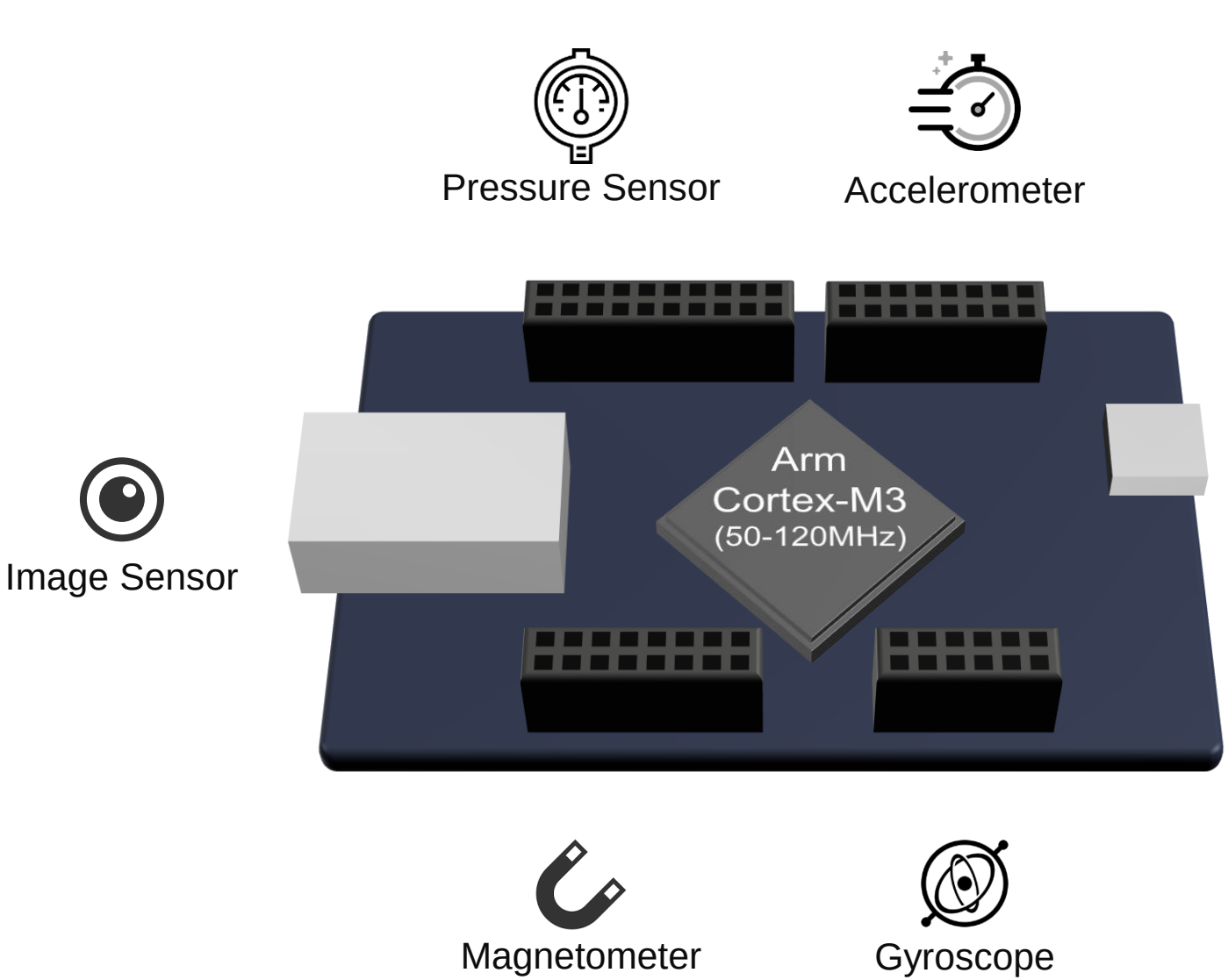
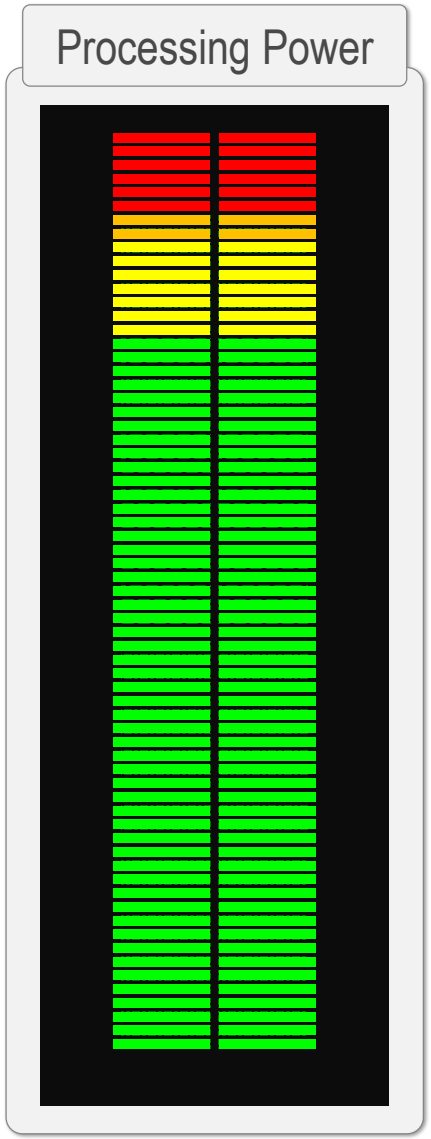
Low Cost ASSPs Provide Limited Interfaces





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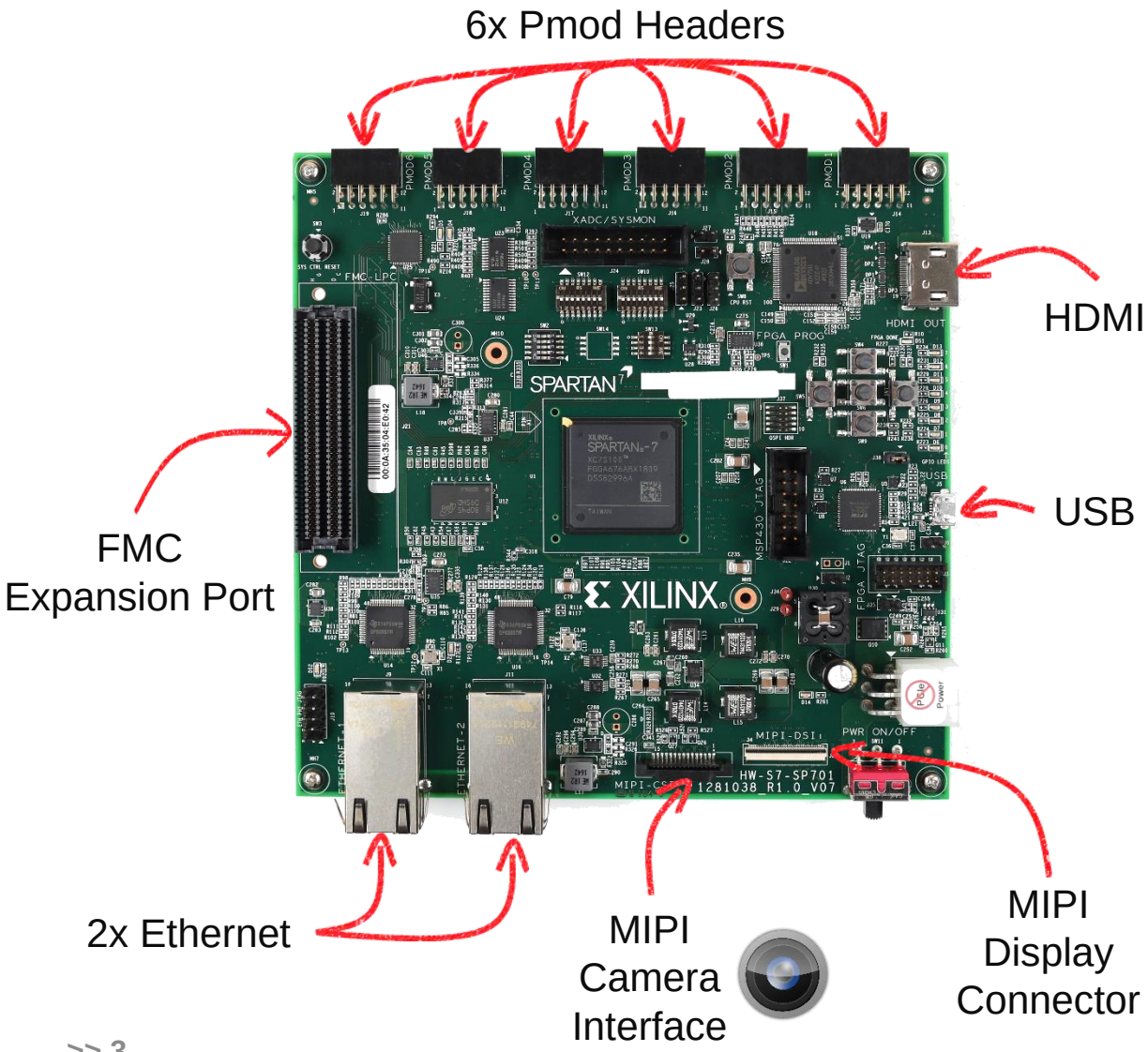
SP701: The King of Sensor Fusion

All the Interfaces Needed to Support Sensor Fusion Development



Over **150** Pmod Sensors Available

Motor Control

Temperature

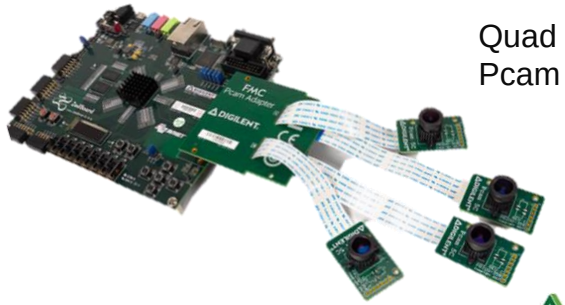
Humidity

Acceleration

Gyroscope

Altitude

Over **100** FPGA Mezzanine Cards Available



Quad Camera
Pcam Adapter

DIGILENT
A National Instruments Company

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Spartan®-7: The Most Capable Cost-Optimized FPGA

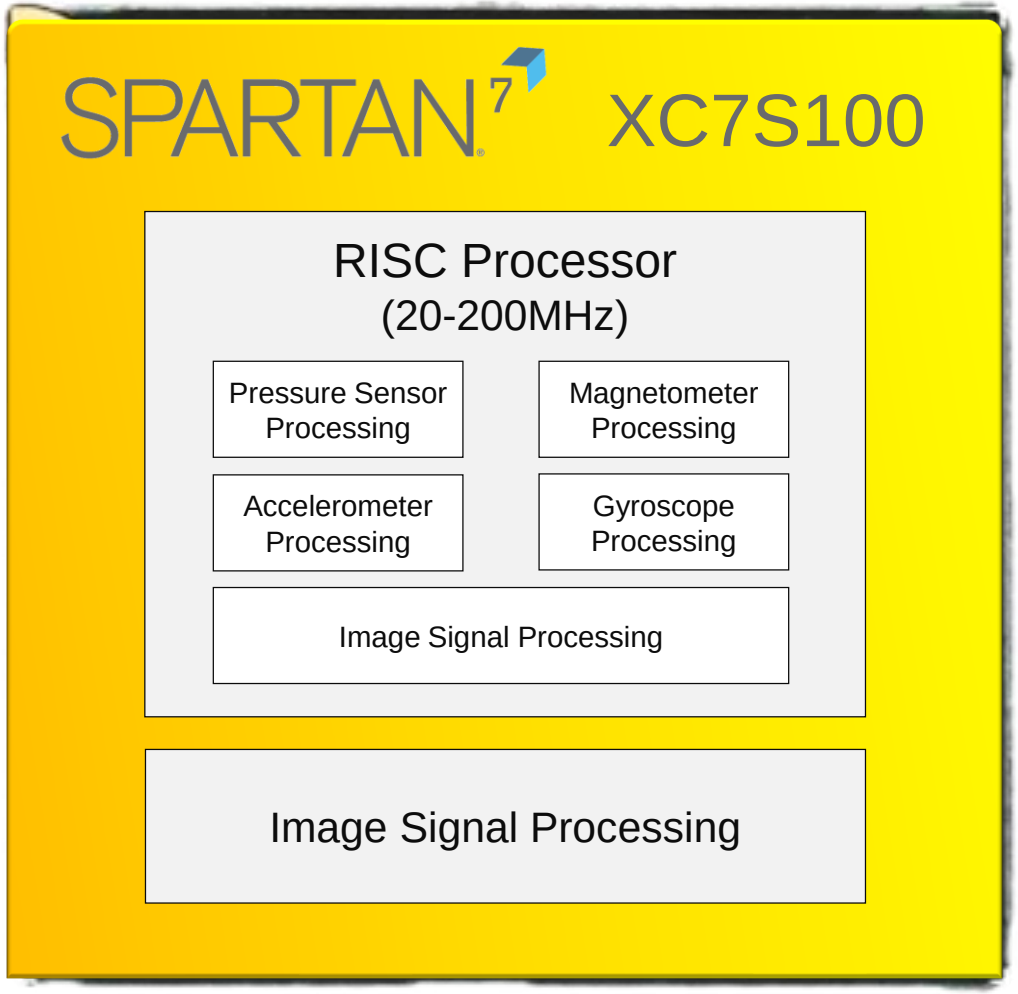
Pressure Sensor

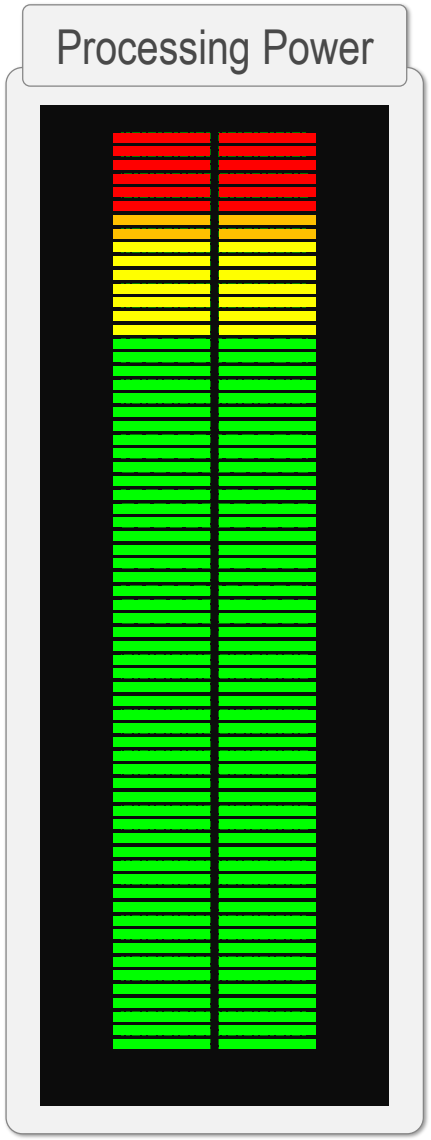
Accelerometer

Magnetometer

Gyroscope

Image Sensor





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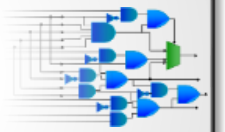
Spartan®-7 FPGA Overview

2.5X Perf/Watt

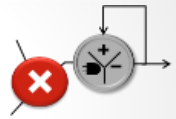
50% lower power and 30% faster than previous generation



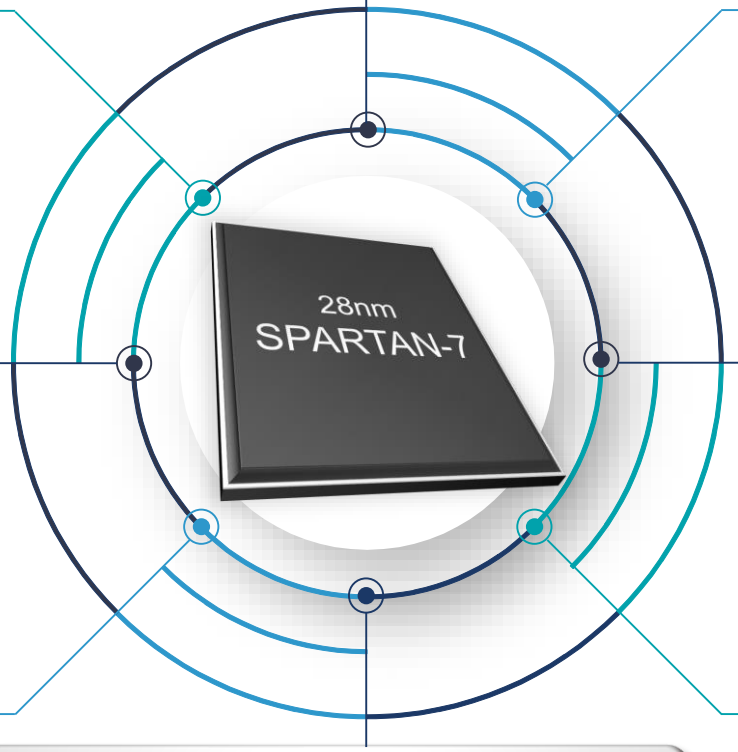
Internal Memory

- Up to 4.2Mb total
- Perfect for code storage & clock domain crossing, FIFOs

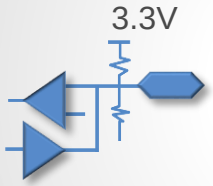
DSP



- Wide 25x18 MACs
- Up to176GMACs for DSP and Image Filters especially video motion estimation

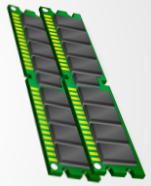


Flexible I/O



- Any-to-Any Connectivity
- Up to 1.25G LVDS
- Up to 400 I/O

External Memory



- Support for DDR3-800, DDR2, LPDDR2 up to 1GB densities

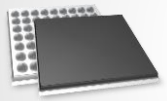
Security

- Encryption & Authentication
- AES256 CBC & SHA-256

ADC & System Monitor

- Dual 12-bit 1MSPS ADC with 17 input Analog Mux
- Thermal monitoring

Small Form Factor



Only 28nm device in an 8x8mm package with 100 I/O

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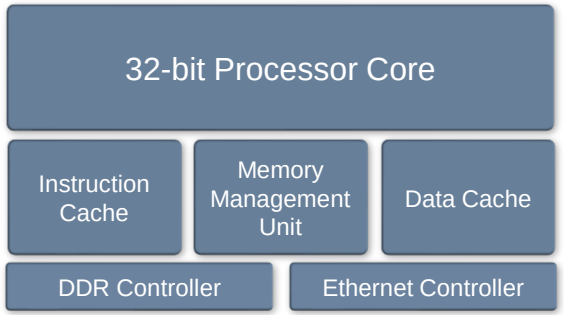
Easily Implement MicroBlaze or Arm Cortex-M Processors

MicroBlaze



- 32-bit RISC Processor @ up to 200MHz
  - 64-bit version available also available
- Three prebuilt MicroBlaze Presets
  - Application Processor running Linux
  - Real-Time Processor running FreeRTOS
  - Microcontroller with Bare Metal
- Free, native Vitis Support with no licensing free

arm Cortex-M

- World's most popular microcontroller
  - Massive ecosystem of tools and libraries
- Arm® Cortex™-M1 & M3 running up to 100MHz
  - Instant download, no license fees
- Keil MDK support
- DesignStart FPGA Program

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Add as Many Peripherals as You Want

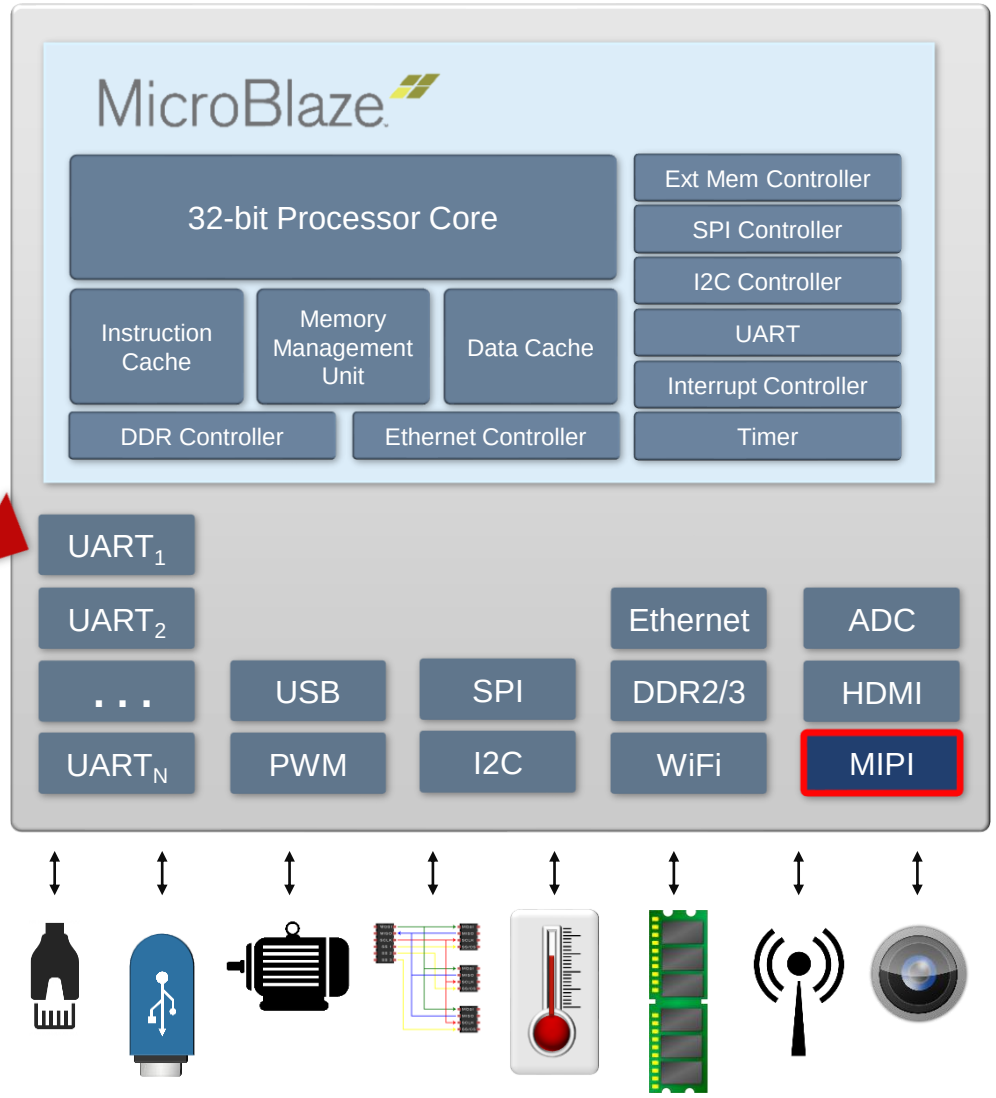
Expand and "Future-Proof" Your System for the Latest Standards

Drag, Drop from
100's of IP & Peripherals

- IP Catalog
  - Partner IP
  - Automotive & Industrial
    - CAN
    - . . .
  - Embedded
  - Networking
  - Video & Image Processing
  - Digital Signal Processing

. . .

Drag, Drop, and Customize



- ✓ **Expand** interfaces and feature set as requirements change
- ✓ Adopt the **latest protocols** *(e.g., EtherCAT, TSN, …)*
- ✓ "**Future-Proof**" your system against evolving standards

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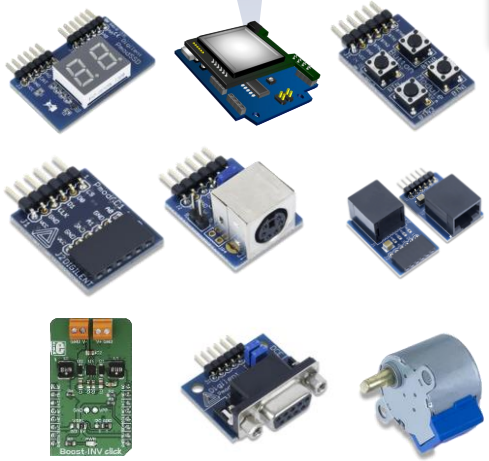
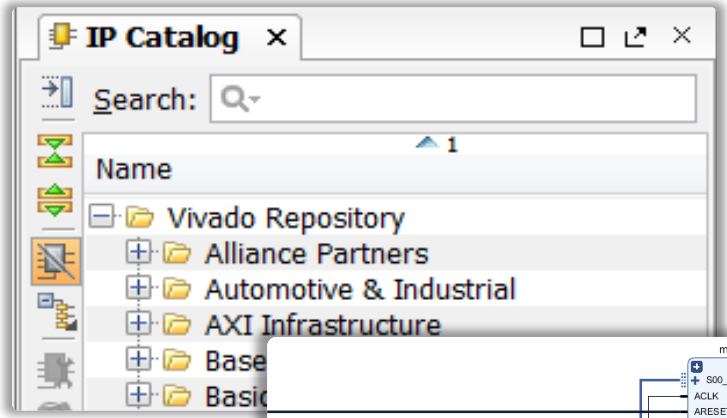
Drag and Drop Any Peripheral You Need

Select from Catalog

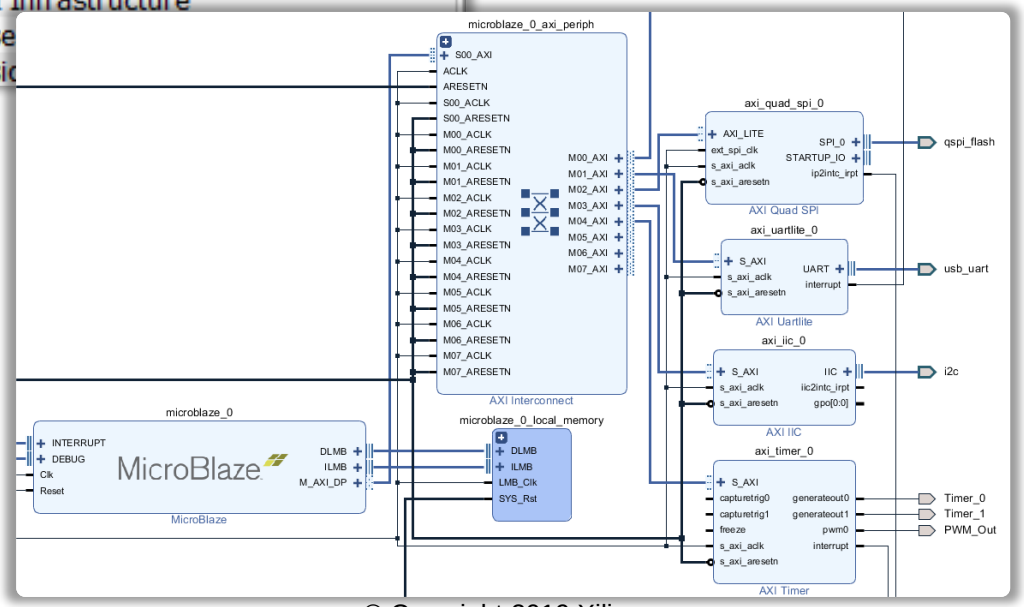
IP Peripheral

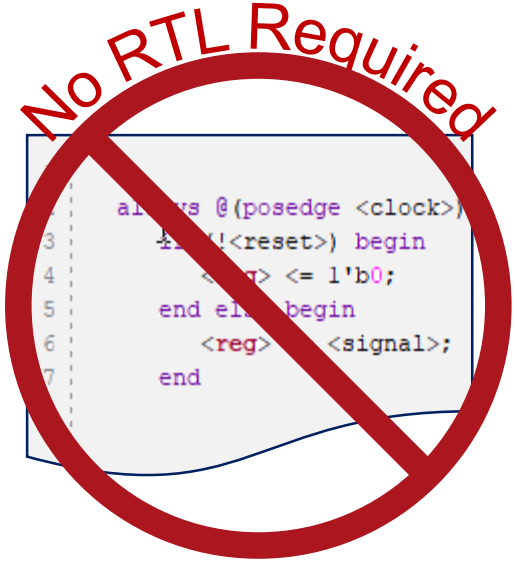
Select from 100s of PMODs





Drag & Drop Into Design





Rapid Bring-Up in Hardware

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So How Do We Offload Image Signal Processing?

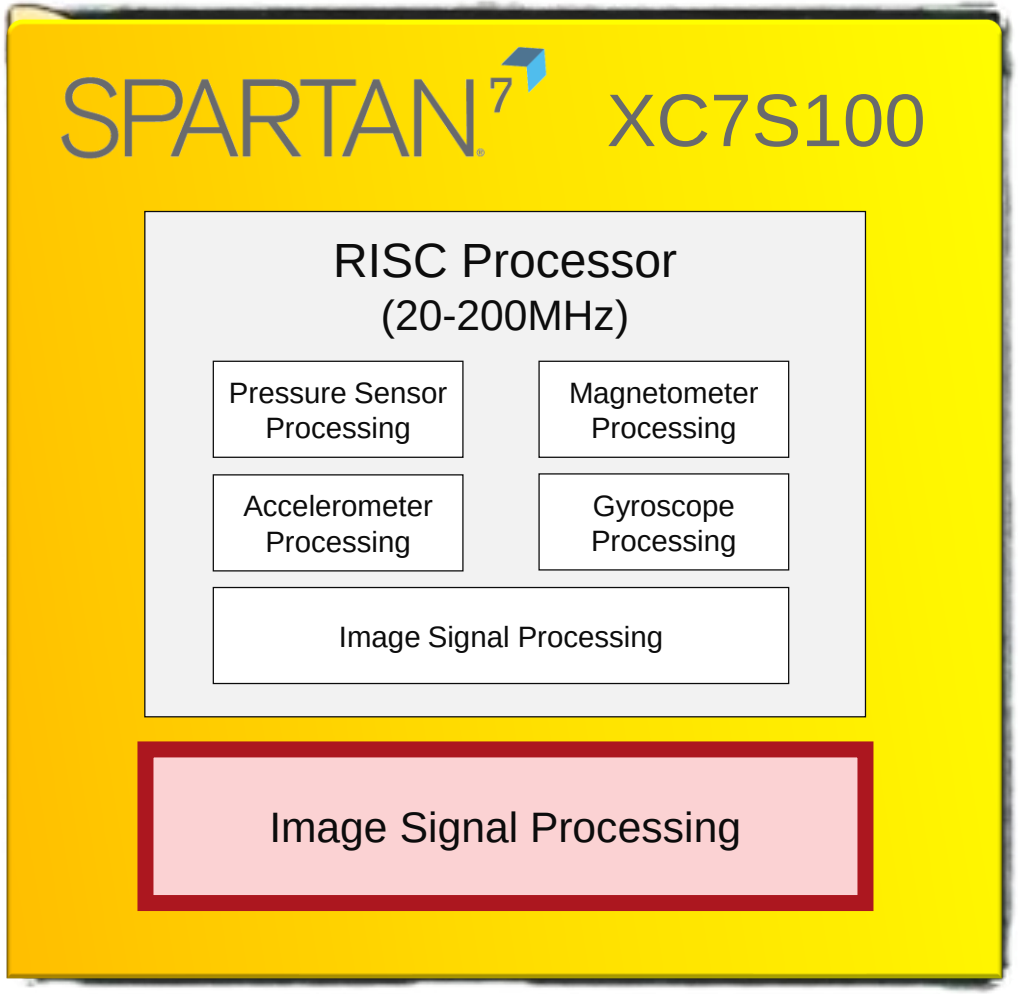
Pressure Sensor

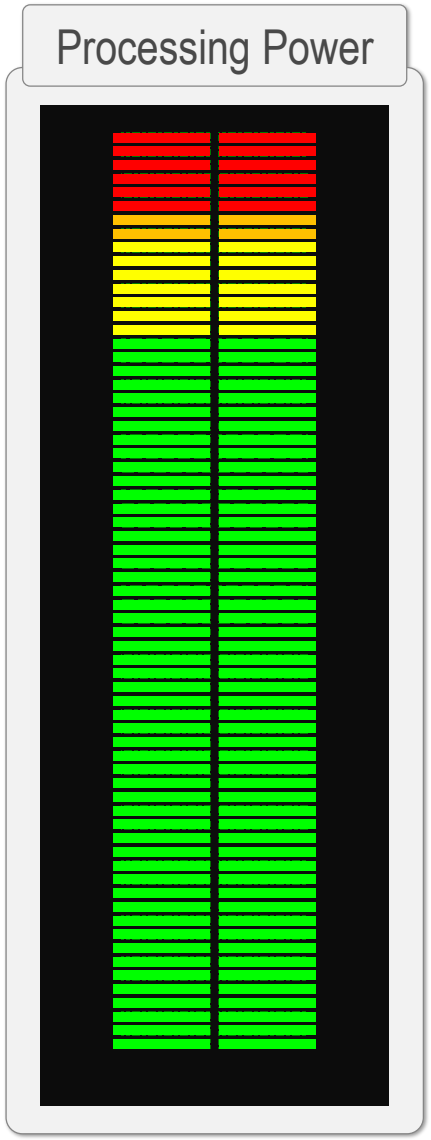
Accelerometer

Magnetometer

Gyroscope

Image Sensor





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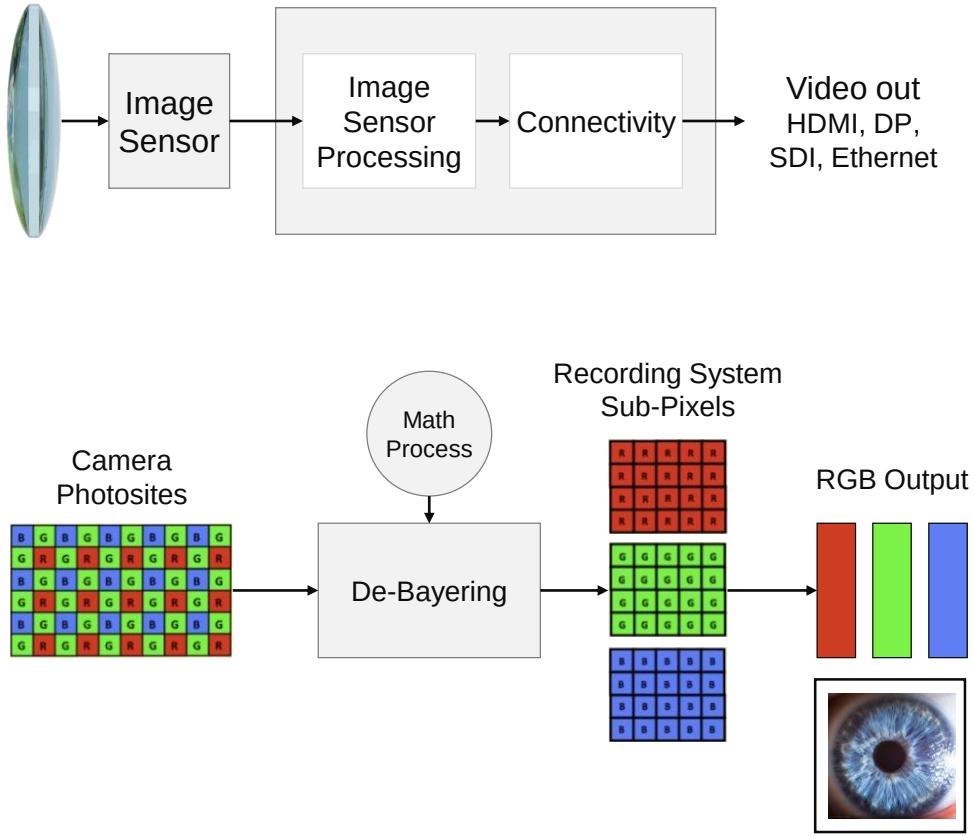
First…What is Image Sensor Processing?

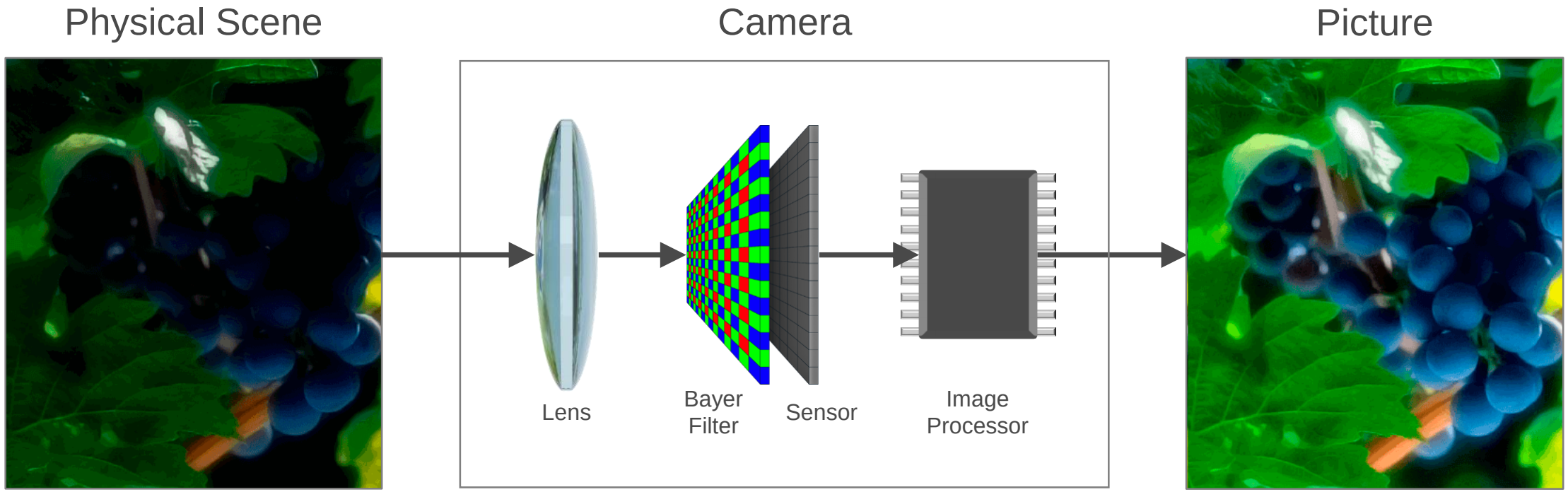
- Modern day sensors capture images with only one color/pixel called Raw or Bayer images
- To reconstruct the image, Image Sensor Processors (ISP) interpolate the values of three primary colors (RGB) for each pixel using a Debayer function
  - Debayer is also called Demosaic and is the minimum function required of an ISP
- Additional ISP image enhancement functions include:
  - Noise reduction
  - Stuck pixel correction
  - 3A algorithm to adjust for light conditions
  - Gamma and Color correction



Bayer image → ISP → RGB image

What are Image Signal Processors?

ISPs Transform Raw Image Sensor Output to a Usable Picture



Why Do You Need Image Signal Processing?

- All ISPs have tradeoffs according to application
  - Mobile Phone ISPs are designed to enhance human attractiveness in Selfies
  - Traditional DSLR ISPs are optimized to produce images for a variety of Subjects
  - Automotive ISPs are designed to deal with difficult lighting conditions
  - PC and Tablet ISPs are designed for video conferencing

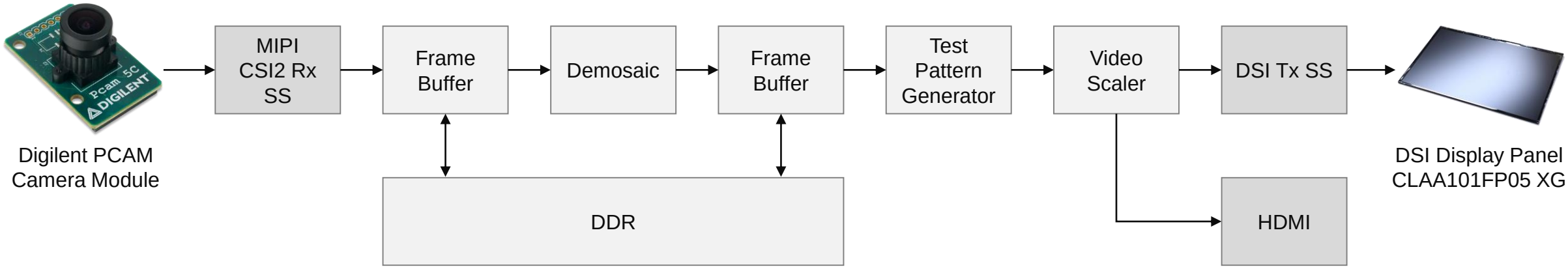
- Using an ISP intended for another application further degrades performance
  - ISPs manipulate Image Data to produce Images that appear more suitable for the task
  - Color manipulations
  - Local & Global tone mapping
  - Skin Smoothing
  - Sky Enhancements
  - And more..

ISP Functions from Xilinx

- Demosaic (Debayer), Color Correction and Gamma LUT
  - Used for reconstructing raw images to RGB or YUV images (PG286 and PG285)
  - Does not include advanced functions such as 3A algorithm, Noise reduction
  - Comes with both Linux and Bare metal drivers
- Showcased in several example designs:
  - Spartan SP701 example design
  - MIPI Design example generated in Vivado
  - reVISION Reference designs
- Other ISP solutions from partners:
  - Xylon, Regulus, A2E, Pinnacle, OCAM ISP from Core-cam

Spartan 701 MIPI Example Design

- Example Design Features:
  - CSI-2 Subsystem IP with PCAM camera module (Digilent)
    - Popular interface used by MIPI CSI camera modules
  - DSI Subsystem IP with display (CLAA101FP05 XG)
    - 1920x1200 RGB3
  - DPHY implementation using XAPP894 using passive components
  - MicroBlaze control of CSI and DSI
- Integrated and delivered as Vivado example design in 2019.2



Sensor Fusion Demo

Spartan-7 SP701 Evaluation Kit

Designed for Edge Applications Requiring Multiple Sensors and High I/O

Evaluate Spartan-7 7S100 capabilities

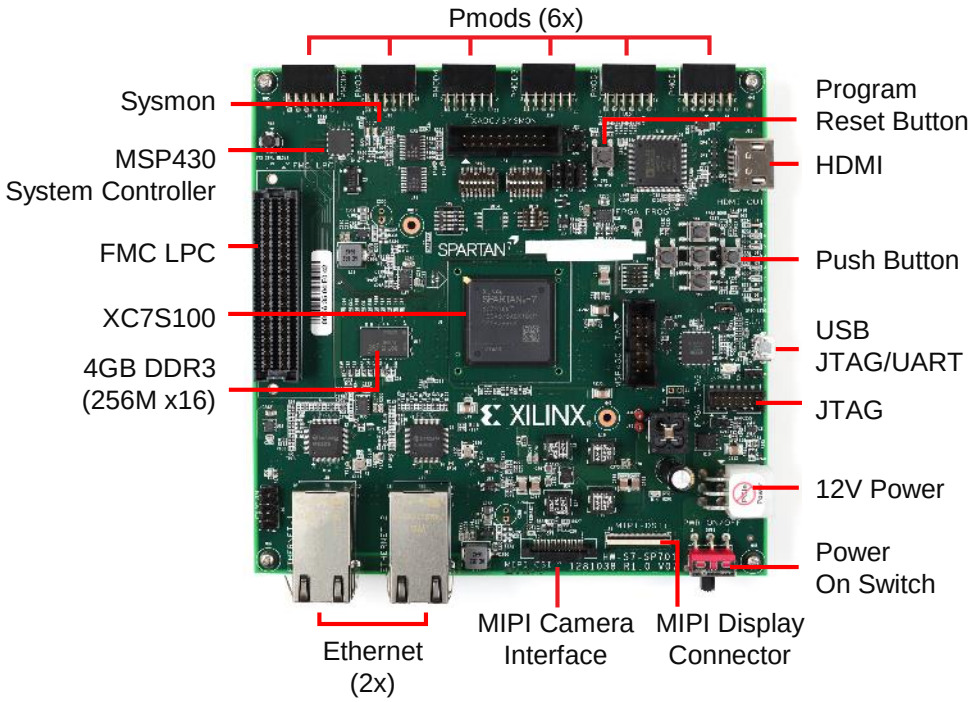
- Largest Spartan-7 device with 102K LUTs
- Over 350 of the 400 I/O pins mapped to the SP701
- Scalable across the industry's broadest Cost-Optimized Portfolio

Develop for sensor heavy applications

- Video interfaces including MIPI CSI, DSI, and HDMI
- Expandable I/O via Pmods and FMC interfaces
- Dual ethernet for industrial networking

Leverage extensive IP development canvas

- Pre-configured MicroBlaze™ processor example designs
- Arm® Cortex®-M1 and Cortex-M3 DesignStart FPGA available



Ordering Information	
Part Number:	EK-S7-SP701-G
Price:	$645
Availability:	Now
www.xilinx.com/sp701	

Summary

- The SP701 Evaluation Kit with the Spartan-7 FPGA is ideal for rapid prototyping of sensor fusion applications
  - Includes abundant high speed inputs
  - Xilinx FPGAs are infinitely flexible
  - FPGA architecture is suited to image processing
  - Allows custom pixel packing for simplicity versus power consumption
  - Integrated design scalers and I/O resources in a single chip
- Vast ecosystem of plug and play sensor modules are available
- With Xilinx embedded processors and Vivado, start interfacing with sensors in minutes!

- Calls to action
  - Visit the www.xilinx.com/sp701 and buy a board to try it yourself
  - Schedule a visit from your local FAE or sales representative for a demo

Adaptable.
Intelligent.

MIPI DPHY and IP Solutions Matrix

	Spartan-7	Artix-7	Kintex-7	Zynq-7000	Zynq UltraScale+
MIPI D-PHY	External D-PHY chip or XAPP894	External D-PHY chip or XAPP894	External D-PHY chip or XAPP894	External D-PHY chip or XAPP894	Native IO support
MIPI DSI / Host (TX) IP Provider	Xilinx NWL	NWL Xilinx	NWL Xilinx	NWL Xilinx	Xilinx NWL
MIPI DSI / Peripherals (RX) IP Provider		NWL	NWL	NWL	NWL
MIPI CSI2 / RX IP provider	Xilinx NWL	NWL Xilinx	NWL Xilinx	NWL Xilinx	Xilinx NWL
MIPI CSI2 / TX IP provider	Xilinx NWL	NWL Xilinx	NWL Xilinx	NWL Xilinx	Xilinx NWL

- D-PHY Data rates using XAPP 894 are limited to </= 800Mbps.
- D-PHY Data rates using external D-PHY chip vary by device
- D-PHY Data rates in 16-nm US+ devices are expected to run up to 2500Mbps;

FPGA Advantages in Image Signal Processing

Architecturally Advantageous

- Abundant high speed inputs for higher resolution data rates
- Allows custom pixel packing to improve power consumption
- Low latency

Infinitely Flexible

- Create and test custom algorithms quickly and easily
- Use the right image processing for the application

Integrated Design Scalers

- Resolution scaling for application specific needs
- Multiple video compressors for streaming video