Secure Digital Card Series, Min.32MB ~ Max.512MB
SD & SPI Interface Mode

GENERAL DESCRIPTION

SD Memory Card (Secure Digital Memory Card) is a memory card that is specifically designed to meet the security, capacity, performance and environment requirements inherent in newly emerging audio and video consumer electronic devices. The SD Memory Card will include a copyright protec-tion mechanism that complies with the security of the SDMI standard and will be faster and capable for higher Memory capacity. The SD Memory Card security system uses mutual authentication and a "new cipher algorithm" to protect from illegal usage of the card content. A none secured access to
the user' s own content is also available. The physical form factor, pin assignment and data transfer protocol are forward compatible with the MultiMediaCard with some additions.

The SD Memory Card communication is based on an advanced 9-pin interface (Clock, Command, 4xData and 3xPower lines) designed to operate in at maximum operating frequency of 25MHz of and low voltage range. The communication protocol is defined as a part of this specification. The SD Memory Card host interface supports regular MultiMediaCard operation as well. In other words, MultiMediaCard forward compatibility was kept. Actually the main difference between SD Memory Card and MultiMediaCard is the initialization process.

FEATURES

- Targeted for port able and stationary applications
- Voltage range :
  SD Memory Card -
  Basic communication (CMD0, CMD15, CMD55, ACMD41): 2 .0 - 3 .6 V
  Other commands and memory access : 2.7 - 3.6 V
- SDLV Memory Card (low voltage) - Operating voltage range : 1.6 - 3.6 V
- Designed for read-only and read/write cards.
- Variable clock rate 0-25MHZ
- Up to 10MByte/secRead/Write rate (using 4parallel data lines).
- Maximum data rate with up to 10 cards
- Correction of memory field errors
- Card removal during read operation will never harm the content
- Forward compatibility to Multi Media Card Copy rights Protection Mechanism-Complies with highest security of SDMI standard.
- Password Protection of cards(option)
- Write Protect feature using mechanical switch
- Built -in write protection features (permanent and temporary)
- Card Detection (Insertion/Removal).
- Application specific commands
- Comfortable erase mechanism
- Protocol attributes of the communication channel :
  SD Memory Card Communication Channel
  Six-wire communication channel (clock, command, 4 data lines)
  Error-protected data transfer
  Single or Multiple block oriented data transfer
- SD Memory Card thickness is defined as either 2.1mm (normal) and 1.4mm (Thin SD Memory Card).

PRODUCT SPECIFICATIONS

Capacities :

32, 64, 128, 256 and up to 512 MB (formatted)

System Compatibility :

Please refer to the compatibility list of index.

Performance :

Host Data Transfer Rates : Up to 10MByte/secRead/Write rate (using 4parallel data lines).

Operating Voltage : 2.7V ~3.6V

Environment conditions :

1) Standard Operation Conditions

Absolute Maximum Temperature Range: Ta = -25 to +85 degrees centigrade
(Humidity less than RH = 95 %, Non condensed)

Recommended Operating Conditions: Ta = 0 to +55 degrees centigrade
(Humidity RH = 20% to 85 % Non condensed)

Note :

Absolute maximum temperature range shows the maximum range which can operate in some condition, and DOES NOT mean a guaranteed operation in any conditions.
For the Stable operations, the recommended operating conditions are suggested or please ask for the customized conditions to HANBiT sales representatives.

2) Storage Temperature

Absolute Maximum Temperature Range: Tstg = -40 to +85 degrees centigrade
(Humidity less than RH = 95% Non condensed)

Recommended Storage Conditions: Tstg = -20 to +65 degrees centigrade
(Humidity RH = 5% to 85% Non condensed)

Note :

Absolute maximum temperature range shows the maximum range to store.
However, DOES NOT mean a guaranteed conditions for long term.
There are some impacts on the SD card if stored in this temperature rage for long term.
For the long term storage period, the recommended storage conditions is suggested
or please ask for the customized conditions to HANBiT sales representatives.

Interface(SD Physical Layer Specification Ver.1.0 Compliant)

SD Card Interface, (SD: 4 or 1bit)

SPI Mode Compatible

- Compliant with PHYSICAL LAYER SPECIFICATION Ver.1.0. (Part1)
- Compliant with FILE SYSTEM SPECIFICATION Ver.1.0. (Part2)
- Compliant with SECURITY SPECIFICATION Ver.1.0. (Part3)

DC Characteristics:

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage 1		V_{DD}	-	2.0	-	3.6	V	For CMD0, 15,55, ACMD41 Only
Supply Voltage 2			-	2.7	-	3.6	V	For All commands
Input Voltage	High Level	V_{IH}	-	VDD*0.625	-	-	V	
	Low Level	V_{IL}	-	-	-	VDD*0.25	V	
Output Voltage	High Level	V_{OH}	VDD = 2V IOH = -100uA	VDD*0.75	-	-	V	
	Low Level	V_{OL}	VDD = 2V IOL = 100uA	-	-	VDD*0.125	V	
Standby Current		I_{CC1}	3.6V Clock 25MHz	-	-	30	mA	
			2.7V Clock Stop	-	-	0.2		
Operation Voltage		I_{CC2}	3.6V/25MHz	-	-	80	mA	Write
			2.7V/25MHz	-	-	80		Read
Input Voltage Setup Time		Vrs	-	-	-	250	ms	

AC Characteristics:

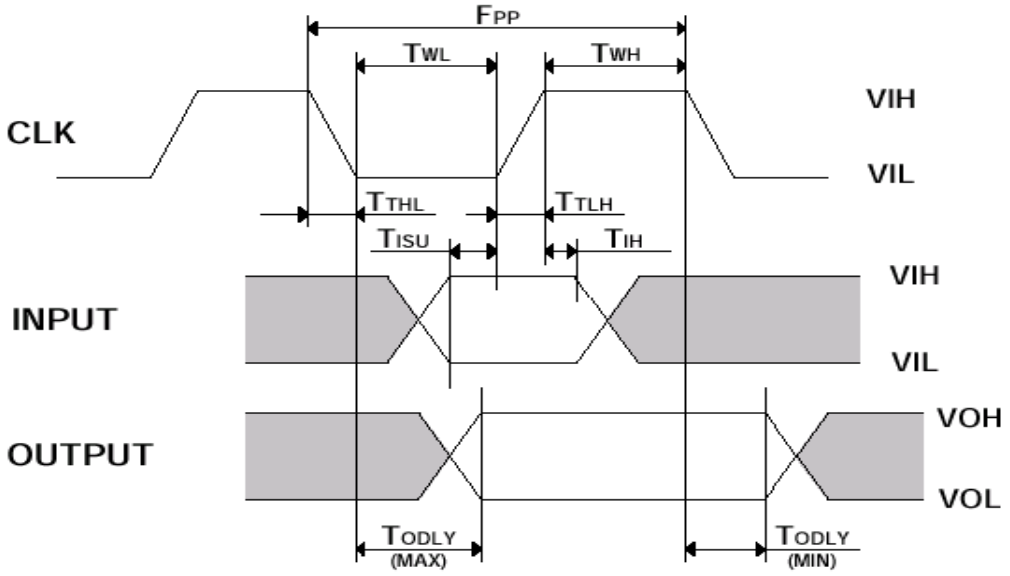
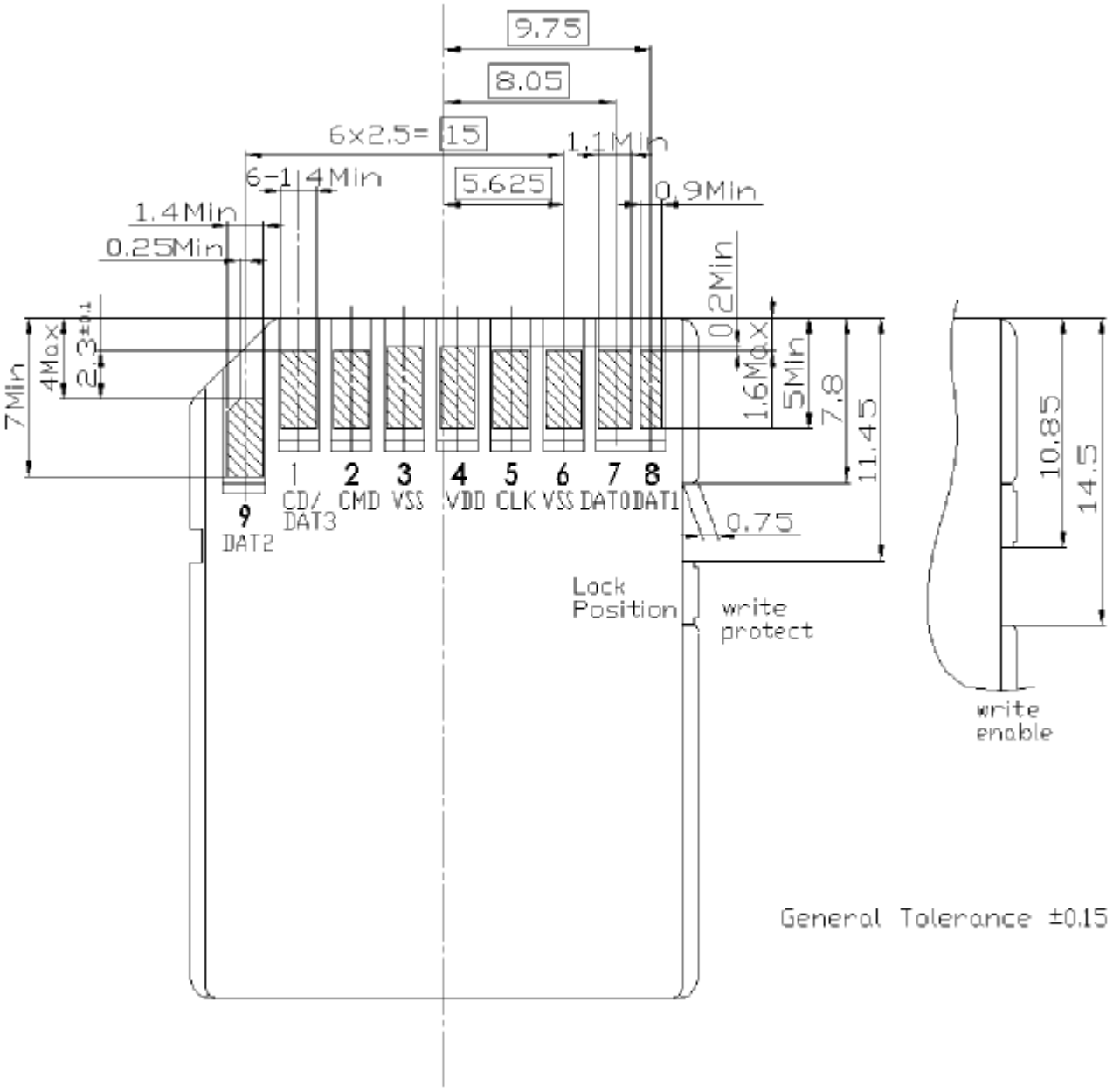


Fig : AC Timing Diagram

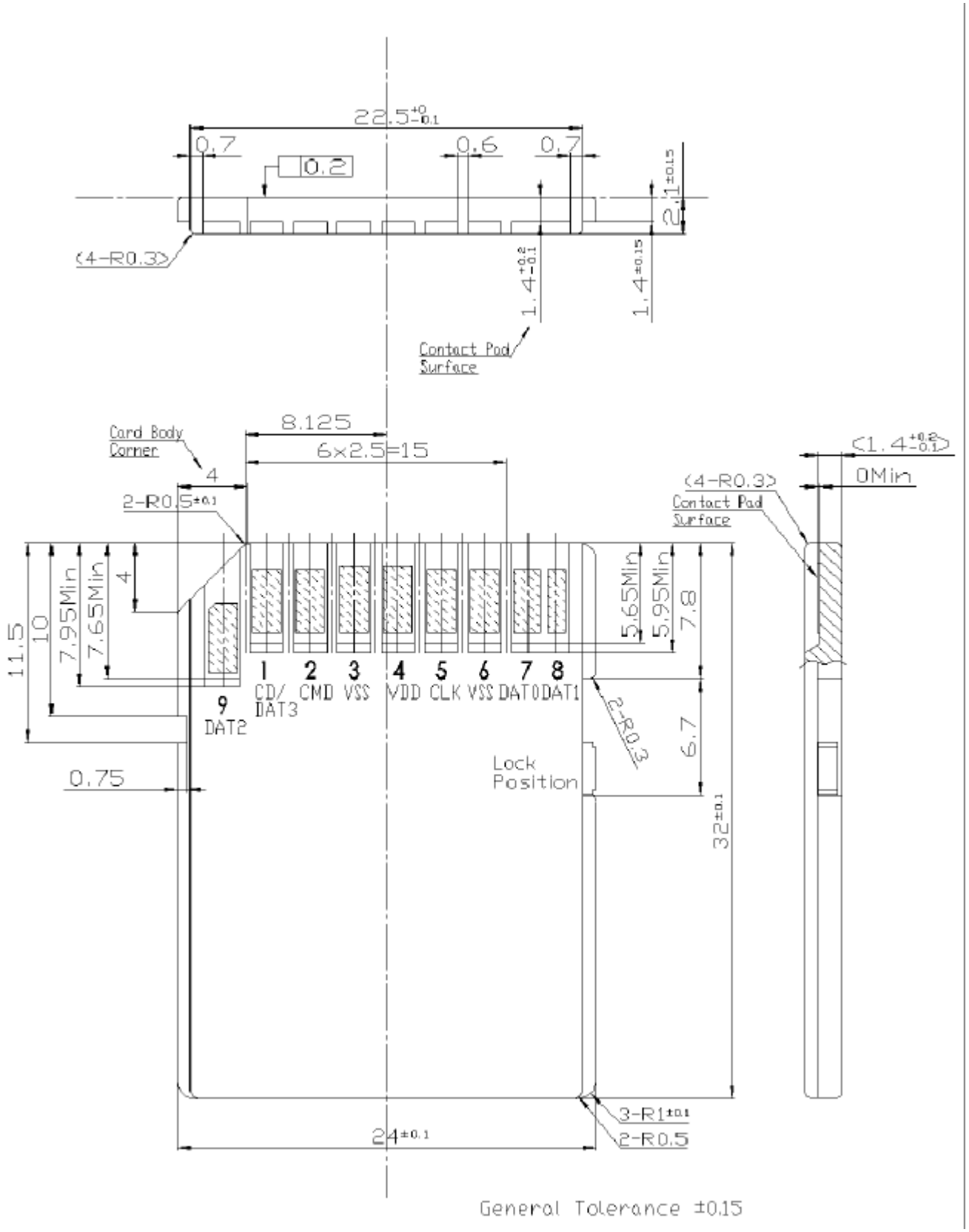
Table : AC Characteristics

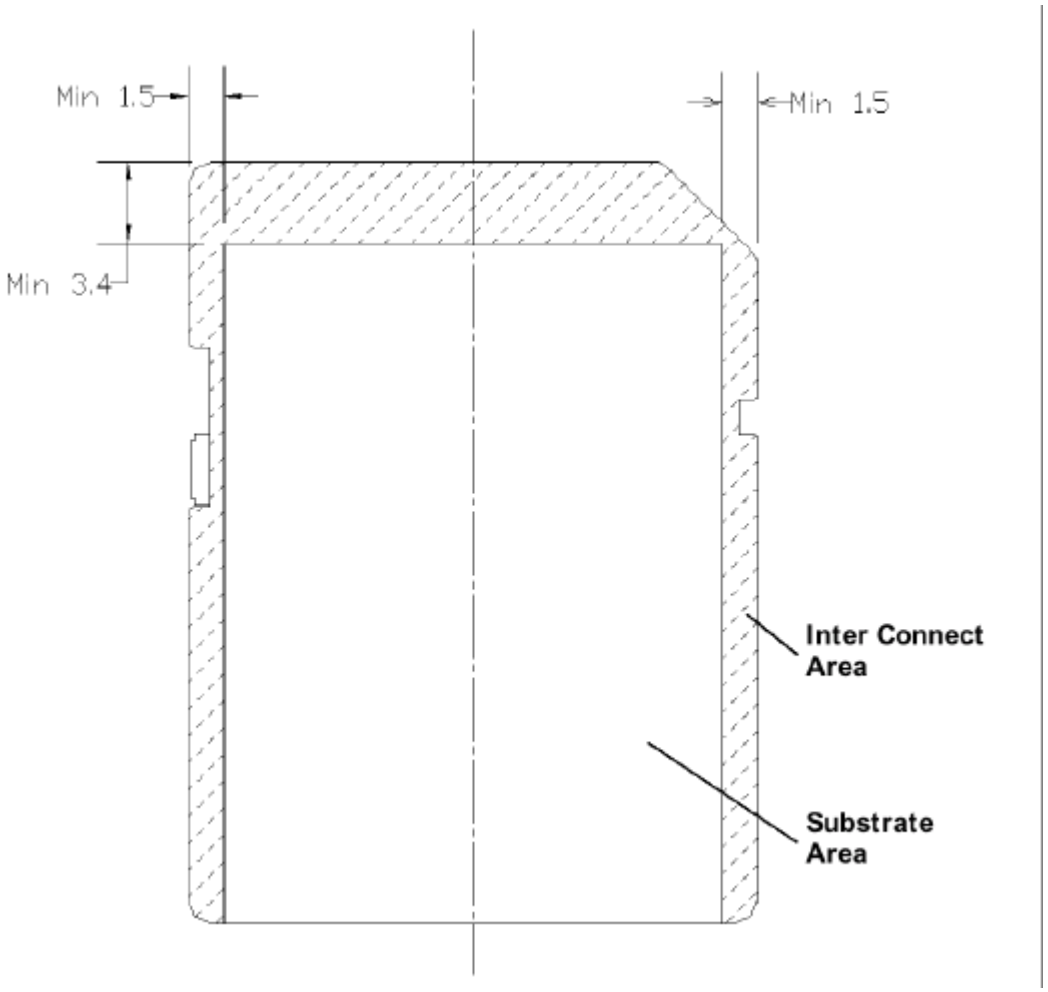
Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any Sates)	F_{sty}	0	25	MHz	C_L<100pF (7Cards)
Clock Frequency (Data transfer Mode)	F_{PP}	0.1	25	MHz	C_L<100pF (7Cards)
Clock Frequency (Card identification Mode)	F_{OD}	100	400	kHz	C_L<250pF (21Cards)
Clock Low Time	T_{WL}	10	-	ns	C_L<100pF (7Cards)
Clock High Time	T_{WH}	10	-	ns	
Clock Rise Time	T_{TLH}	-	10	ns	
Clock Fall Time	T_{THL}	-	10	ns	
Clock Low Time	T_{WL}	50	-	ns	C_L < 250pF (21Cards)
Clock High Time	T_{WH}	50	-	ns	
Clock Rise Time	T_{TLH}	-	50	ns	
Clock Fall Time	T_{THL}	-	50	ns	
Input Setup Time	T_{ISU}	5	-	ns	C_L < 25pF (1Cards)
Input Hold Time	T_{IH}	5	-	ns	
Output Delay Time	T_{ODLY}	0	14	ns	

PHYSYCAL SPECIFICATION



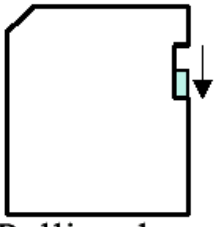
Weight	2.0 g. maximum
Length:	32mm ± 0.1mm
Width:	24mm ± 0.1mm
Thickness:	2.1mm ± 0.15mm (in substrate area only, 2.25mm maximum)


22.5+0 -0.1
0.7
0.6
0.7
0.2
2.1±0.15
(4-R0.3)
1.4+0.2 -0.1
1.4±0.15
Contact Pad Surface
Card Body Corner
8.125
6×2.5=15
4
2-R0.5±0.1
(1.4+0.2 -0.1)
0Min
(4-R0.3)
Contact Pad Surface
11.5
10
7.95Min
7.65Min
4
5.65Min
5.95Min
7.8
1 CD/DAT3
2 CMD
3 VSS
4 VDD
5 CLK
6 VSS
7 DAT0
8 DAT1
9 DAT2
2-R0.3
6.7
Lock Position
0.75
32±0.1
3-R1±0.1
2-R0.5
24±0.1
General Tolerance ±0.15



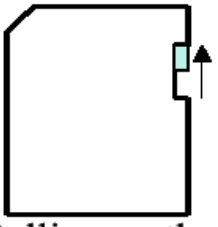
- **R/W card(WP switch is movable)**

Write unable

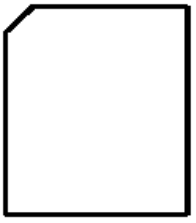


Pulling down the WP Switch.

Write enable

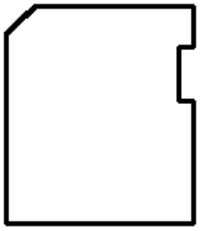


Pulling up the WP Switch.



This is the case of 1.4mm card which does not support the WP switch.

- **ROM card(WP area is fixed)**



This form is same as taking off the WP Switch from R/W card.

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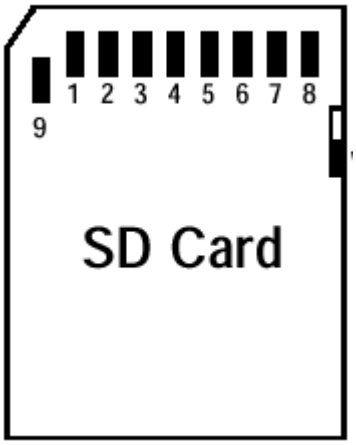
PIN ASSIGNMENTS AND PIN TYPE

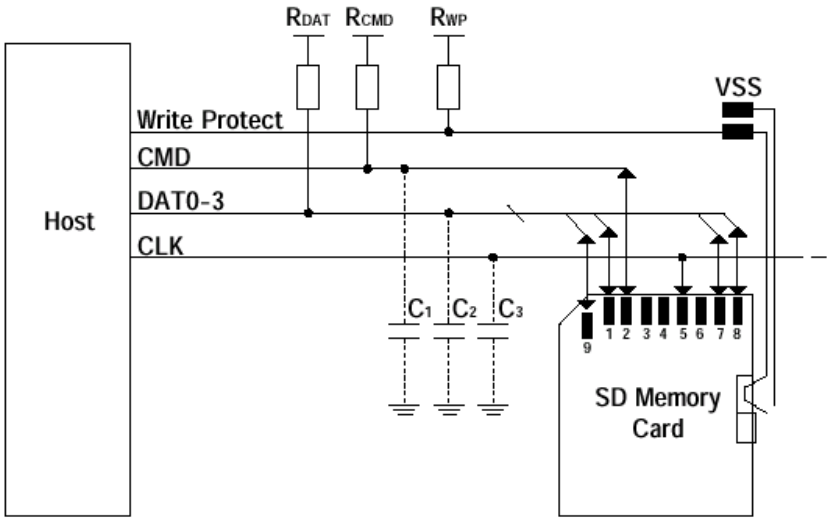


SD Card Pin assignment (Back view of the Card)

Pins	SD Mode			SPI Mode		
	Name	IO type [1]	Description	Name	IO Type	Description
1	CD/ DAT3	I/O /PP	Card Detect/ Data Line [Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Ground	V_{SS}	S	Ground
4	V_{dd}	S	Supply Voltage	V_{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O /PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line [Bit1]	RSV	-	Reserved (*)
9	DAT2	I/O /PP	Data Line [Bit2]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally,‘ PP’ - IO using push-pull drivers

2) (*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.



SD CARD BUS TOPOLOGY AND REGISTERS

- SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width. Multiplied SD cards connections are available to the host. Common V_{dd}, V_{ss} and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.

This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card.

Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:

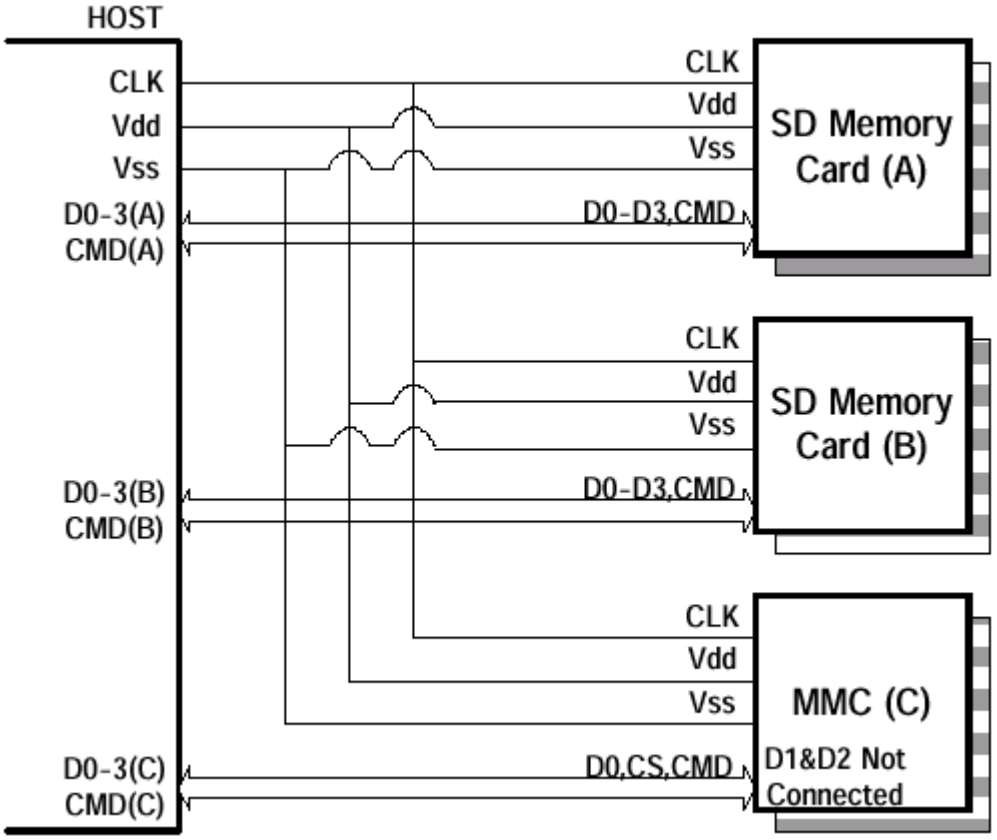
Responses are transferred serially on the CMD line.

A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data can be transfer from the card to the host or vice versa.

Data is transferred via the data lines.



SD Card (SD Mode) connection Diagram

CLK : Host card Clock signal

CMD : Bi-directional Command/ Response Signal

DAT0 - DAT3: 4 Bi-directional data signal

V_{dd} : Power supply

V_{ss} : GND

SD Mode Command Set

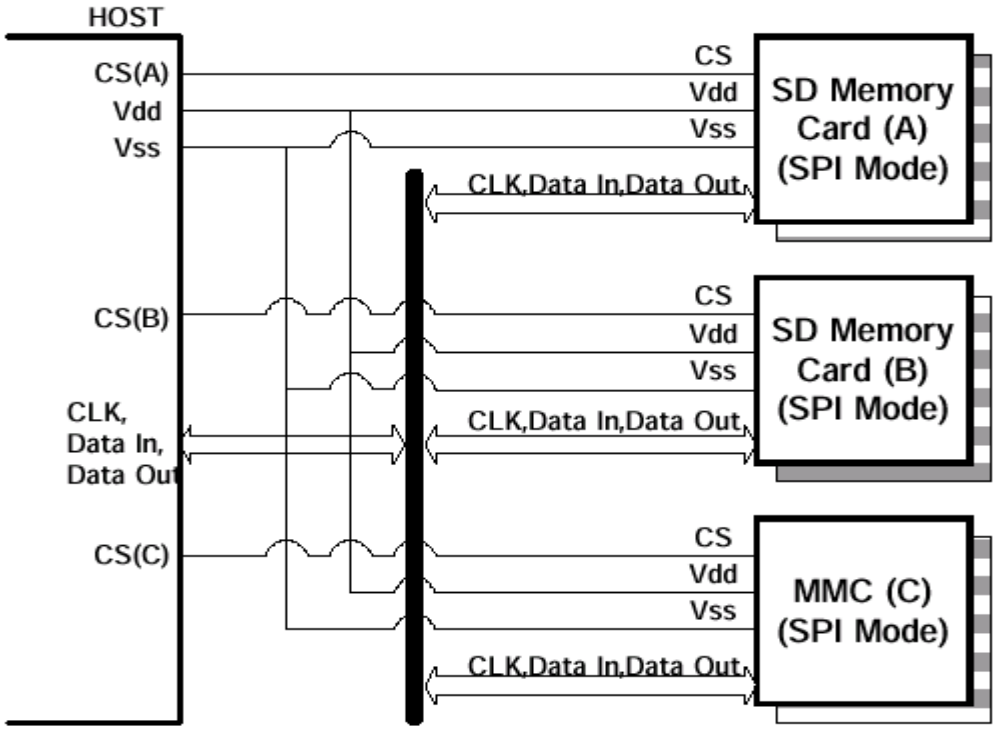
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD7	SELECT/DESELECT_CARD	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	-	Card Lock/Unlock Function is not implemented.
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29,30 and CMD42 are Optional Commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is for vender specific command. Which is not defined in the standard card.

SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).
The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.
All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.
The advantage of the SPI mode is reducing the host design in effort.
Especially, MMC host can be modified with little change.
The disadvantage of the SPI mode is the loss of performance versus SD mode.
Caution: Please use SD Card Specification. DO NOT use MMC Specification.
For example, initialization is achieved by ACMD41, and be careful to Register. : GND Register definition is different, especially CSD Register.



SD card (SPI mode) connection diagram

CS: Card Select Signal — CLK: Host card Clock signal
Data in: Host to card data line — Data out: card to host data line
Vdd : Power supply — Vss : GND

SPI Bus Mode Pad Definition

Pin #	Name	Type[1]	SPI Description
1	CS	I	Chip Select (Active low)
2	DataIn	I	Host to Card Commands and Data
3	VSS1	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	CLK	I	Clock
6	VSS2	S	Supply Voltage Ground
7	DataOut	O	Card to Host Data and Status
8	RSV(2)	I	Reserved
9	RSV(2)	I	Reserved

NOTES: 1) S=power supply; I=input; O=output.
2) The 'RSV' pins are floating inputs. It is the responsibility of the host designer to connect external pullup resistors to those lines. Otherwise non-expected high current consumption may occur due to the floating inputs.

SPI Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 and 9.2)
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	-	Card Lock/Unlock Function is not implemented.
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

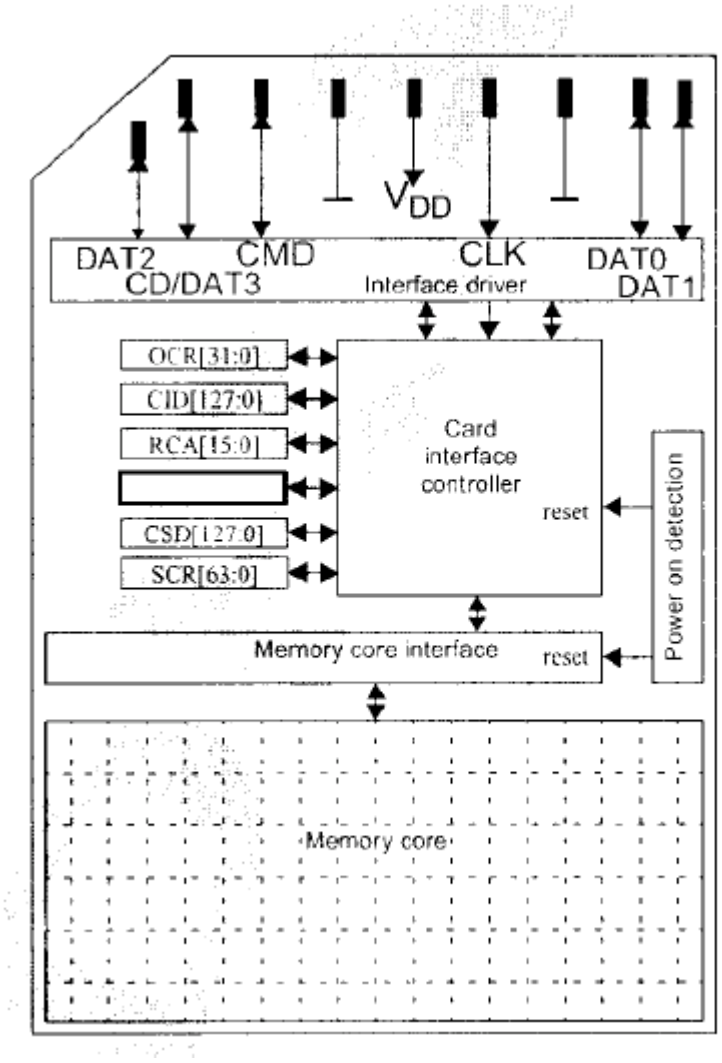
- CMD28, 29,30 and CMD42 are Optional Commends.
- CMD56 is for vender specific command. Which is not defined in the standard card.

SD Card Registers

Name	Width	Description
CID	128	Card identification number: individual card number for identification.
RCA[1]	16	Relative card address: local system address of a card, dynamically suggested by the card and approved by the host during initialization.
CSD	128	Card specific data: information about the card operation conditions.
SCR	64	SD Configuration Register: information about the SD Card's special features capabilities.
OCR	32	Operation Condition Register

NOTE: 1) The RCA register is not available in SPI Mode.

The host may reset the cards by switching the power supply off and on again. The card has its own power-on detection circuitry which puts the card into an idle state after the power-on. The card can also be reset by sending the GO_IDLE (CMD0) command.



There is a set of seven registers within the card interface. The OCR, CID, CSD and SCR registers carry the card configuration information. The RCA register holds the card relative communication address for the current session. The card status and SD status registers hold the communication protocol related status of the card.

Operating Conditions Register (OCR)

Accessing the data in the memory array, however, requires 2.7 to 3.6 Volts. The OCR shows the voltage range in which the card data can be accessed. The structure of the OCR register is described in next table.

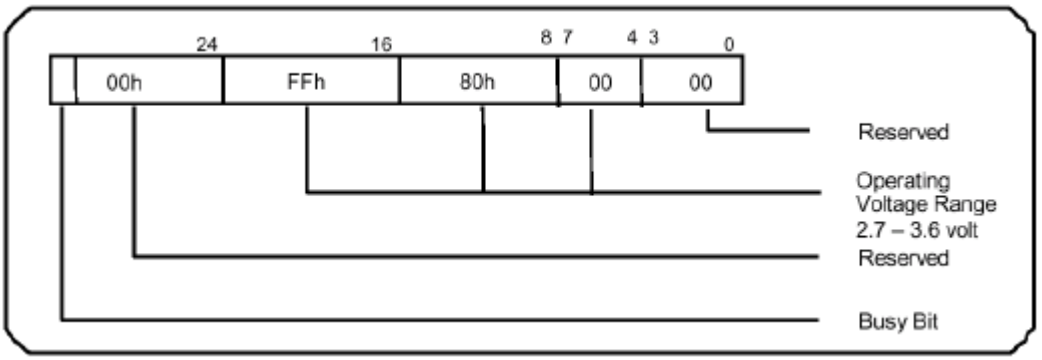
OCR Bit	VDD Voltage Window
0-3	Reserved
4	1.6-1.7
5	1.7-1.8
6	1.8-1.9
7	1.9-2.0
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9

OCR Bit	VDD Voltage Window
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-30	reserved
31	Card power up status bit (busy)

The level coding of the OCR register is as follows:

Restricted voltage windows=LOW
Card busy=LOW (bit 31)

The least significant 31 bits are constant and will be set as described in this figure. If bit 32 (the busy bit) is set, it informs the host that the card power up procedure is finished.



Card Identification (CID) Register

The CID register is 16 bytes long and contains a unique card identification number as shown in next table. It is programmed during card manufacturing and cannot be changed by SD Card hosts. Note that the CID register in the SD Card has a different structure than the CID register in the MultiMediaCard.

Name	Type	Width	CID—Slice	Comments	CID Value
Manufacturer ID (MID)	Binary	8	[127:120]	The manufacturer IDs are controlled and assigned by the SD Card Association.	0x03
OEM/Application ID (OID)	ASCII	16	[119:104]	Identifies the card OEM and/or the card contents. The OID is assigned by the 3C.*	SD ASCII Code 0x53, 0x44
Product Name (PNM)	ASCII	40	[103:64]	5 ASCII characters long	SD128, SD064, SD032, SD016, SD008
Product Revision** (PRV)	BCD	8	[63:56]	Two binary coded decimal digits	Product Revision (30)
Serial Number (PSN)	Binary	32	[55:24]	32 Bits unsigned integer	Product Serial Number
Reserved		4	[23:20]		
Manufacture Date Code (MDT)	BCD	12	[19:8]	Manufacture date–yym (offset from 2000)	Manufacture date(for example: Apr 2001 = 0x014)
CRC7 checksum*** (CRC)	Binary	7	[7:1]	Calculated	CRC7
Not used, always '1'		1	[0:0]		

* 3C = The 3 SDA founding companies: Toshiba, SanDisk, and MEI.

** The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and the "m" is the least significant nibble. Example: The PRV binary value filed for product revision "6.2" will be: 0110 0010.

*** The CRC Checksum is computed by the following formula:
CRC Calculation: G(x)=x7+3+1
M(x)=(MID-MSB)*x119+...+(CIN-LSB)*x0
CRC[6...0]=Remainder[(M(x)*x7)/G(x)]

CSD Register

The Card Specific Data (CSD) register contains configuration information required to access the card data. In this table 3-10, the cell type column defines the CSD field as Read only (R), One Time Programmable (R/W) or erasable (R/W/E). This table shows the value in "real world" units for each field and coded according to the CSD structure. The Model dependent column marks (with a check mark, √) the CSD fields that are model dependent.
Note that the CSD register in the SD Card has a different structure than the CSD in the MultiMediaCard.

Name	Field	Width	Cell Type	CSD-Slice	CSD Value	CSD Code
CSD structure	CSD_STRUCTURE	2	R	[127:126]	1.0	00b
Reserved	-	6	R	[125:120]	-	000000b
data read access-time-1	TAAC Binary MLC	 8 8	 R R	 [119:112] [119:112]	 1.5msec 10msec	 00100110b 00100110b
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0	00000000b
max. data transfer rate	TRAN_SPEED	8	R	[103:96]	25MHz	00110010b

Name	Field	Width	Cell Type	CSD-Slice	CSD Value	CSD Code
card command classes	CCC	12	R	[95:84]	All (incl. WP, Lock/unlock)	1F5h
max. read data block length	READ_BL_LEN	4	R	[83:80]	512byte	1001b
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	Yes	1b
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	No	0b
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	No	0b
DSR implemented	DSR_IMP	1	R	[76:76]	No	0b
Reserved	-	2	R	[75:74]	-	00b
device size	C_SIZE	12	R	[73:62]	SD128=3843 SD064=3807 SD032=1867 SD016=899 SD008=831	F03h EDFh 74Bh 383h 33Fh
max. read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]	25mA	100b
max. read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]	25mA	011b
max. write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]	25mA	100b
max. write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]	35mA	100b
device size multiplier	C_SIZE_MULT	3	R	[49:47]	SD128=64 SD064=32 SD032=32 SD016=32 SD008=16	100b 011b 011b 011b 010b
erase single block enable	ERASE_BLK_EN	1	R	[46:46]	Yes	1b
erase sector size	SECTOR_SIZE	7	R	[45:39]	32blocks	0011111b
write protect group size	WP_GRP_SIZE	7	R	[38:32]	128sectors	1111111b
write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	Yes	1b
Reserved for MultiMediaCard compatibility		2	R	[30:29]	-	00b
write speed factor Binary MLC	 R2W_FACTOR R2W_FACTOR	 3 3	 R R	 [1:16] [1:4]	 X16 X16	 100b 010b
max. write data block length	WRITE_BL_LEN	4	R	[25:22]	512Byte	1001b
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	No	0
Reserved	-	5	R	[20:16]	-	00000b
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]	0	0b
copy flag (OTP)	COPY	1	R/W(1)	[14:14]	Not Original	1b
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	Not Protected	0b
temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	Not Protected	0b
File format	FILE_FORMAT	2	R/W(1)	[11:10]	HD w/partition	00b
Reserved		2	R/W	[9:8]	-	00b

Name	Field	Width	Cell Type	CSD-Slice	CSD Value	CSD Code
CRC	CRC	7	R/W	[7:1]	-	CRC7
not used, always'1'	-	1	-	[0:0]	-	1b

NOTE: The device size indicates the user area size. It does not include the protected area that is used for security applications and is about 1 percent of the total card size.

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

SCR Register

In addition to the CSD register, there is another configuration register that is named SD CARD Configuration Register (SCR). SCR provides information on SD Card's special features that were configured into the given card. The size of SCR register is 64 bit. This register shall be set in the factory by the SD Card manufacturer. Table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice	SCR Value	SCR Code
SCR Structure	SCR_STRUCTURE	4	R	[63:60]	V1.0	0
SD Card—Spec. Version	SD_SPEC	4	R	[59:56]	V1.01	0
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]	0	0
SD Security Support	SD_SECURITY	3	R	[54:52]	Prot 2, Spec V1.01	2
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]	1 & 4	5
Reserved	-	16	R	[47:32]	0	0
Reserved for manufacturer usage	-	32	R	[31:0]	0	0

Status Register

The SD Card supports the following two card status fields:

Card Status—This status field is compatible to the MultiMediaCard protocol.

SD Status—This extended status field of 512 bits supports special features unique to the SD Card and future application specific features.

The SD Card status registers' structures are defined in next table. The Type and Clear-Condition fields in the table are coded as follows:

Type:

E—Error bit.

S—Status bit.

R—Detected and set for the actual command response.

X—Detected and set during command execution. The host must poll the card by sending status command in order to read these bits.

Clear Condition:

A—According to the card current state.

B—Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).

C—Clear by read.

Bits	Identifier	Type	Value	Description	Clear Cond.
31	OUT_OF_RANGE	E R X	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	E R	'0'= no error '1'= error	A misaligned address that did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R	'0'= no error '1'= error	The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E R X	'0'= no error '1'= error	An invalid selection of write-blocks for erase occurred.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	Attempt to program a write-protected block.	C
25	CARD_IS_LOCKED	S X	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A
24	LOCK_UNLOCK_FAIL ED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/ unlock card command or if there was an attempt to access a locked card	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card state	B
21	CARD_ECC_FAILED	E R X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E R X	'0'= no error '1'= error	Internal card controller error	C
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
18	Reserved				
17	Reserved				
16	CID/ CSD_OVERWRITE	E R X	'0'= no error '1'= error	Can be either one of the following errors: - The CID register has been already written and can not be overwritten - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
15	WP_ERASE_SKIP	S X	'0'= not protected '1'= protected	Only partial address space was erased due to existing write protected blocks.	C
14	CARD_ECC_DISABLE D	S X	'0'= enabled '1'= disabled	The command has been executed without using the internal ECC.	A
13	ERASE_RESET	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received.	C

Bits	Identifier	Type	Value	Description	Clear Cond.
12:9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data 6 = rcv 7 = prg 8 = dis 9-15 = reserved	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	'0'= not ready '1'= ready	Corresponds to buffer empty signalling on the bus.	A
7:6					
5	APP_CMD	S R	'0' = Disabled '1' = Enabled	The card will expect ACMD, or indication that the command has been interpreted as ACMD.	C
4	Reserved				
3	AKE_SEQ_ERROR (SD Card Security spec.)	E R	'0' = no error '1' = error	Error in the sequence of authentication process.	C
2	Reserved for application specific commands				
1, 0	Reserved for manufacturer test mode				

SD Status

The SD Status contains status bits that are related to the SD Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512 bits. The content of this register is transmitted to the Host over the DAT bus along with 16 bits CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran_state' (card selected). The SD Status structure is listed in Table 3-29. The same abbreviations for ' type' and ' clear condition' were used as for the Card Status above.

Bits	Identifier	Type	Value	Description	Clear Cond.
511: 510	DAT_BUS_WIDTH	S R	'00'=1 (default) '01'=reserved '10'=4 bit width '11'=reserved	Shows the currently defined data bus width that was defined by the SET_BUS_WIDTH command.	A
509	SECURED_MODE	S R	'0'=not in the mode '1'=in secured mode	Card is in Secured Mode of operation (refer to the SD Security Specifications document).	A
508: 496	Reserved				
495: 480	SD_CARD_TYPE	S R	'00xxh'=SD Memory Cards as defined in Physical Spec. Ver. 1.01 ('x'=don't care). The following cards are currently defined: '0000'=Regular SD RD/WR Card. '0001'=SD ROM Card	In the future, the 8 LSBs will be used to define different variations of an SD Card (each bit will define different SD types). The 8 MSBs will be used to define SD Cards that do not comply with the SD Memory Card as defined in the Specification Ver. 1.01	A
479: 448	SIZE_OF_PROTECTED_AREA	S R	Size of protected area (in units of MULT*BLOCK_LEN refer to CSD register.	Shows the size of the protected area. The actual area = (SIZE_OF_PROTECTED_AREA) * MULT * BLOCK_LEN.	A
447: 312	Reserved				
311: 0	Reserved for Manufacturer				

RCA Register

The 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure.

CARD INITIALIZE

To initialize the HANBiT SD card, follow the following procedure is recommended example.

1) Supply Voltage for initialization.

   Host System can apply the Operating Voltage from initialization to the card. Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

   In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to "Low" level. Then, issue CMD0.

   In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to "High" normally).

   Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.

4) Apply the indicated operating voltage to the card.

   Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared.

   (Bit 31 Busy = 1) If response time out occurred, host can recognize not SD Card.

   Note: In MMC-SPI Mode, CMD1 can use in this state.

   However, do not use CMD1 in case of SD Mode.

5) Issue the CMD2 and get the Card ID (CID).

   Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)

6) Issue the CMD7 and move to the transfer state.

   If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.

7) Issue the ACMD13 and poll the Card status as SD Memory Card. Check SD_CARD_TYPE value. If significant 8 bits are "all zero", that means SD Card. If it is not, stop initialization.

8) Issue CMD7 and move to standby state.

   Issue CMD9 and get CSD.

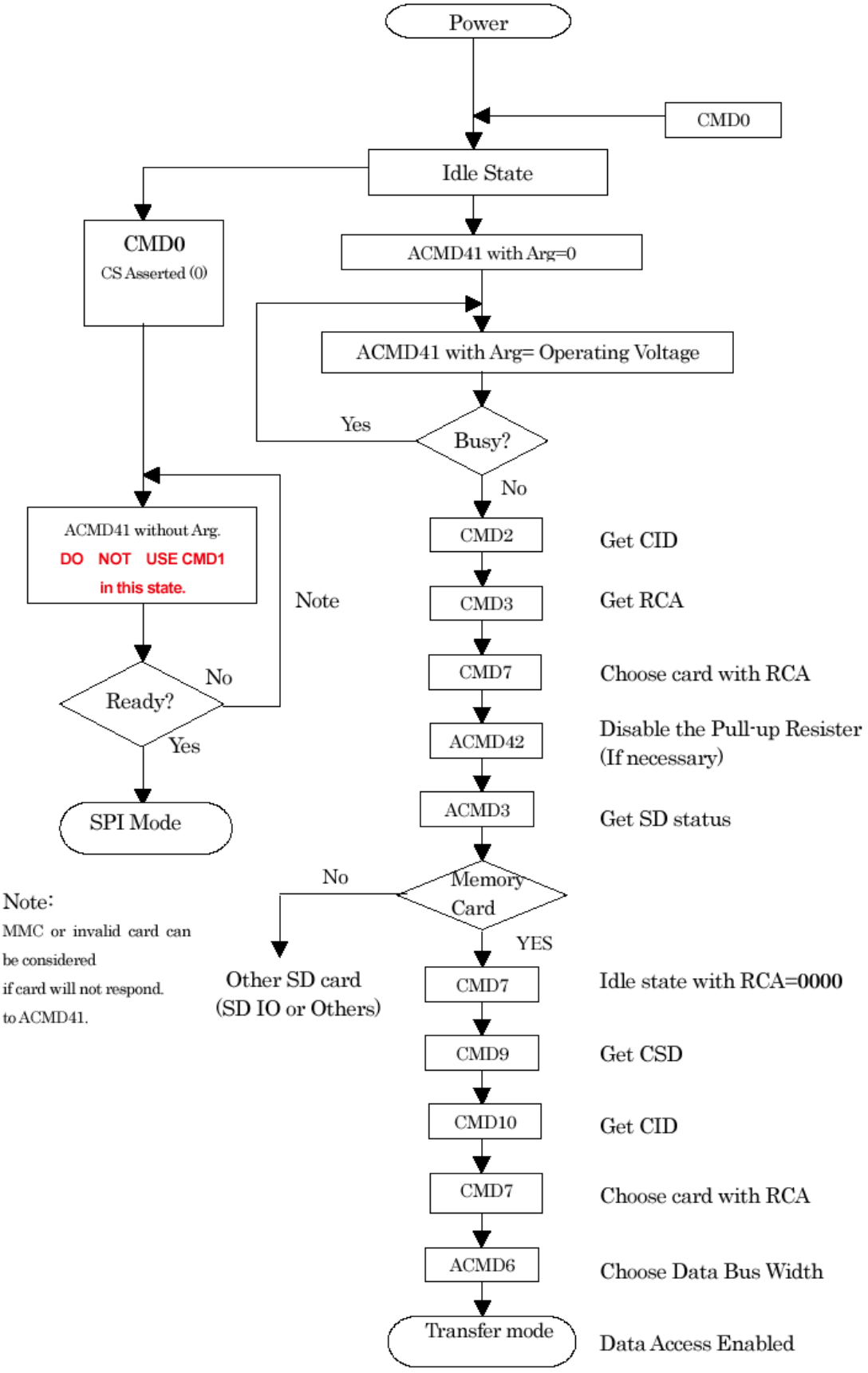
   Issue CMD10 and get CID.

9) Back to the Transfer state with CMD7.

   Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.

Recommended Example of SD card Initialize Procedure



Ordering Infomation

NO	Parts	Capacity	Media transfer mode	Chip Number	Note
1	**SDC-32A**	32Mbyte	BYTE	1	
2	**SDC-64A**	64Mbyte	BYTE	1	
3	**SDC-128A**	128Mbyte	BYTE	1	
4	**SDC-256A**	256Mbyte	BYTE	1	
5	**SDC-512A**	512Mbyte	BYTE	1	