



SIEMENS EDA

PADS™

Release Highlights

Software Version: PADS VX.2.17
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Introduction

This document provides a high-level summary of the PADS VX.2.17 release. Refer to the Release Notes on Support Center for the list of specific known issues and workarounds.

This document includes a summary of the new features in this release. It also includes, if applicable, any authorization code changes required, any major installation changes, and any transitioning issues you should be aware of before installing. Additionally, any last-minute issues found in the final stages of testing are included.

Changes may be added to this document after release. Refer to the Release Highlights document on Support Center for the most up-to-date release information.

New Features Introduced in PADS VX.2.17

This is primarily a release aimed at adding new functionality and fixing customers' logged defects - Service Requests (SRs). The following new products, features, and enhancements are introduced in the PADS VX.2.17 release.

HyperLynx™ AMS

HyperLynx AMS includes the following updates.

Collated DC results from a Monte Carlo analysis

Prior to this release, links to DC results from a Monte Carlo analysis were displayed randomly in the simulation log window. Results were listed based on when and in which processor thread the simulation runs were completed. As an example, thread_0 results might be shown somewhere in the middle of the simulation log, and thread_1 results shown at the end. With the VX.2.17 release, all DC results are collated by processor thread and appear in general chronological order in the simulation log window.

HyperLynx SI/PI/Thermal

This release contains the following improvements along with numerous defect fixes and Security improvements.

HyperLynx LineSim™ Usability Improvements

- Automated interconnect/component grouping for simplified topology visualization
 - Flexible grouping views (connected t-lines, IC's, coupling)
 - Conversion of grouped elements to S-parameter
- Interconnect effects control (short/open individual or groups of elements)
- Symbol selection by net or name searching

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- Cross probing to board from LineSim elements/groups for easy design review
 - S-parameter black box sizing
 - o Automatically sized based on pin/net name information
 - o Improved grid-aligned spacing for wiring
 - S-parameter black box information display
 - o Displays pin and net names from header added during model creation from HyperLynx BoardSim™, LineSim, Advanced Solvers

HyperLynx Package Model Support for Decoupling Analysis

- Enabling easy method to import and incorporate package/die model in post layout
 - o Ability to see effects of the pkg/die/cap models attached to PCB

HyperLynx SI Preview Wizard

- Perform SI design audit
 - o Enables extension of progressive analysis philosophy
 - o Utilize existing simulation method/tech (PRPE)
 - o No vendor IO simulation models needed
- Easily understandable results
 - o Provide more comprehensive results than what currently exists in PRPE
 - o Simplified results presentation for the user
 - o Self-contained detailed HTML report
- Actionable results for physical design improvement
 - o Give user information related to design objects for improving their memory bus design
 - o Reports physical design attributes of nets (#vias, primary route layer, routing lengths) in addition to electrical performance metrics

HyperLynx Power Integrity Setup and Useability

- Pin-grouping at BGAs for DC Drop
 - o Pin groups with total current per group
 - o Assume equipotential at load pins
 - o Enables user to see realistic current distribution
 - o CSV Import and export of pin groups in Pin Group Manager

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- DC Drop reporting and visualization improvements
 - o Performance improvements for large report generation
 - o Each power network report in Summary and Detailed Report tabs with TOC
 - o Easier viewing and comparing reports from DC Drop batch on large number of power networks and top-level pass/fail table for DC Drop batch
 - o New HTML viewer to view the metrics directly from Detailed Report

HyperLynx SERDES

- 200G (IEEE® 802.3dj and OIF CEI) Support
 - o SerDes Compliance Wizard engine updates supporting Maximum Likelihood Sequence Estimation (MLSE) algorithms of COM 4.9
 - o Added Compliance Wizard protocols supporting the latest draft standards:
 - Ethernet 200G KR, CR, C2C, and C2M
 - CEI-224G-LR-PAM4 and CEI-224G-MR-PAM4
- PAMn Support
 - o Needed for USB4 Gen 4 (PAM3)
 - o BoardSim/LineSim integrated support for IBIS-AMI models with IBIS 7.2 PAMn keywords
 - o HTML report and Eye Diagram Viewer updates to measure all eyes with correct labeling
- IBIS-AMI Support Improvements
 - o Integrated IBISCHK parser .ami file checking preventing simulation of AMI models with file errors
 - o Improved AMI output parameter reporting and plotting capabilities
 - o SNR output visualization and SNR-to-BER pass/fail analysis for Alphawave ZeusCORE™ IP
- Updated/Added Compliance Wizard Protocols
 - o CAUI-4-C2M
 - o 25GAUI-C2M/50GAUI-2-C2M/100GAUI-4-C2M/200GAUI-8-C2M/400GAUI-16-C2M
 - o 50GAUI-1-C2M/100GAUI-2-C2M/200GAUI-4-C2M/400GAUI-8-C2M
 - o 100GAUI-1-C2M/200GAUI-2-C2M/400GAUI-4-C2M/800GAUI-8-C2M/1.6TAUI-16-C2M, adding TP1, TP4, and TP4a protocols
 - o CEI-112G-VSR-PAM4
 - o MIPI D-PHY Modes 0-9 and 6G/9G/11G

HyperLynx DRC

The sections below provide details of changes in this version.

Modern UX

Menu cleanup and display improvements.

Use of Constraint and User Areas to define verification regions

- There are two use cases for areas (constraint and other user areas such as KEEPOUT and KEEPIN areas) provided by a design application. These areas define where verification needs to be performed.
- Import “Constraint Areas” from both Xpedition™ and Cadence® Allegro®
- Import “User Areas” from both Xpedition and Cadence Allegro
 - Obstruct areas from Xpedition
 - KEEPOUT & KEEPIN areas from Allegro
 - Ability to apply or ignore rules to these new “Rule Areas”

Creepage Engine Improvements

- New Creepage Wizard will read the Xpedition Constraint Manager data to create the rules for the creepage analysis engine
- Ability to read a CSV file to populate the parameters through the creepage wizard
- Implement the ability to check nets within the same object list
- New AOM methods for the Creepage Engine
- Improved progress bar for Creepage Rules
- Improved accuracy of the Creepage results when path goes over an edge

New Python® module for external automation

- Direct python support – for example: “import HyperLynx DRC” instead of indirectly accessing it through win32com
- Supports the external scripting capabilities on both Windows® and Linux
- Utilize a similar approach to SI/PI bringing commonality to the family of HL products

Other Enhancements and Updates

- Sensor Net Isolation Rule enhancement that will reduce false errors
- In-Group Spacing Rule enhancement that will reduce false errors

Licensing

The PADS VX.2.17 release utilizes the SALT (Siemens Advanced Licensing Technology) MSL software version 4.4.3. that utilizes FlexNet® v11.19.5 *Customers upgrading from previous HyperLynx versions to PADS HyperLynx VX.2.17 must upgrade to this newer version of the Siemens Licensing Server if not already on v4.3 or higher.*

The latest version of licensing software is always available on Account Center:

<https://support.sw.siemens.com/en-US/product/1586485382/downloads>

Authorization Codes

To use PADS VX.2.17, a minimum license version (Exact Access Date) of 2025.09 (September 2025) is required.

You may download your existing authorization codes from Account Center:

<https://account.sw.siemens.com/en-US/licenses>

For additional information on licensing, refer to the *Siemens Digital Industries Software Licensing Manual for Mentor® Products*.

PADS Media Export Compliance

The PADS VX.2.17 release media has an Export Classification Control Number (ECCN) of 3D991.

Support Information

A support contract with Siemens is a valuable investment in your organization's success. With a support contract, you have 24/7 access to the comprehensive and personalized Support Center portal.

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Supported Platforms

Overall Notes

- Specified patches below are minimum levels. Later versions of the patches are valid, supported configurations.
- Except as noted, all products are supported on all platforms.
- Processor and Memory requirements vary based on the mix of applications being used, the design complexity, and infrastructure requirements. Individual needs may vary from those published below.

Processor Note for Intel®/AMD Processors

All Windows OS variants run on Intel or AMD x86 or x64 processors. In the past, the processor GHz speed determined the performance, but recent changes in the internal architecture of both Intel and AMD processors have made these comparisons difficult. Therefore, the following recommendations are being made for all Windows systems:

- Supported processors and systems are those manufactured since 2008 which conform to the subsequent requirements.
- Minimum requirement is a dual-core (or dual processor) system. A quad core is recommended for improved overall system performance. A hyper-threaded processor should be considered a single processor, not a dual processor.
- Intel Celeron® processors are not recommended.
- For best results, maximize processor speed and L1/L2/L3 processor cache memory.
- Typically, cost is the best indicator of performance, and extra investment in processor capability returns better system performance.

File Storage

You can install the libraries and share them for group use across a local area network (LAN). We do not recommend use of shared libraries across a wide area network (WAN) due to issues with latency. Storage of any files on Network Appliance Servers (NAS) are not supported with PADS.

Microsoft® Windows 11

Microsoft Windows 11 (version 22H2 or 23H2, 64-bit), Enterprise Edition and Pro Edition are supported.

While there is no known issue with running Microsoft Windows 11 Home Edition or Educational Edition, the product has not been tested with these editions, and therefore is not supported.

Kernel Configuration: N/A

Processor: Dual-core Intel or AMD processor minimum. See [Processor Note for Intel/AMD Processors](#) above.

Memory: 8GB recommended

Swap Space: 2x the amount of RAM

Windows Server 2022

The following configurations are only supported for the sharing of libraries. All other PADS VX.2.17 products are not supported on any Windows Server platforms:

Microsoft Windows Server 2022 with all current updates via Windows Update.

Processor: Dual-core Intel or AMD processor minimum. See Processor Note for Intel/AMD Processors above.

Memory: 8 GB or more recommended (per simultaneously logged in user)

Swap Space: 2X the amount of RAM

Windows Server 2025

The following configurations are only supported for the sharing of libraries. All other PADS VX.2.17 products are not supported on any Windows Server platforms:

Microsoft Windows Server 2025 with all current updates via Windows Update.

Processor: Dual-core Intel or AMD processor minimum. See Processor Note for Intel/AMD Processors above.

Memory: 8 GB or more recommended (per simultaneously logged in user)

Swap Space: 2X the amount of RAM

Java® Support

The provided version of the Java Runtime Environment is the OpenJDK® 17.0.15_6. The OpenJDK version of Java is free from the licensing restrictions imposed on Oracle® Java versions released after Oracle's change in Java licensing terms in January 2018.

This version of Java is the latest available at the time the contents of this release were established. The Java Runtime Environment is included in the product such that it is only used by Siemens EDA products and such that it does not conflict with any other version of Java installed on the target system. Because this version has been tested for use with the Siemens EDA products, ***replacement of the JRE with any other JRE version is not supported.***