```
1         ----------------------------------------------------------------------------------
2         -- Company: DAMAGE Inc.
3         -- Engineer: MYXATA
4         --
5         -- Create Date:    12:42:48 09/25/2007
6         -- Design Name:
7         -- Module Name:    sum - Behavioral
8         -- Project Name:
9         -- Target Devices:
10        -- Tool versions:
11        -- Description:
12        --
13        -- Dependencies:
14        --
15        -- Revision:
16        -- Revision 0.01 - File Created 25.09.2007
17        -- Additional Comments:
18        --
19        ----------------------------------------------------------------------------------
20        library IEEE;
21        use IEEE.STD_LOGIC_1164.ALL;
22        use IEEE.STD_LOGIC_ARITH.ALL;
23        use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25
26        entity sum_acc is
27            Port (
28                   RST : in  STD_LOGIC;
29                   CLK : in  STD_LOGIC;
30                   STRT_CRC: in STD_LOGIC;
31                   DATA_IN : in  STD_LOGIC_VECTOR (7 downto 0);
32                   CRC_OUT : out  STD_LOGIC_VECTOR (5 downto 0)
33                  );
34        end sum_acc;
35
36        architecture Behavioral of sum_acc is
37
38        signal REG:std_logic_vector(7 downto 0);
39
40        begin
41
42
43        SUM_ACC:process(RST,CLK,DATA_IN,REG)
44        begin
45           if RST = '1' then
46               REG <= "00000000";
47           elsif clk'event and clk = '1' then
48              if STRT_CRC ='1' then
49                 REG <= REG + DATA_IN ;
50              end if;
51           end if;
52        end process SUM_ACC;
53        CRC_OUT <= REG(7 downto 2);
54
55        end Behavioral;
56
57
```