RX Introduction

RX Platform
32bit CISC Microcontroller
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Note:
The mentioned specifications may be subject to change due to product improvements or other reasons.

Content

- RX Introduction
- RX600 Basics and Features
- RX600 Product Groups
- RX Application Examples
- Development Tools

RX Introduction

The RX Platform, as extreme as possible

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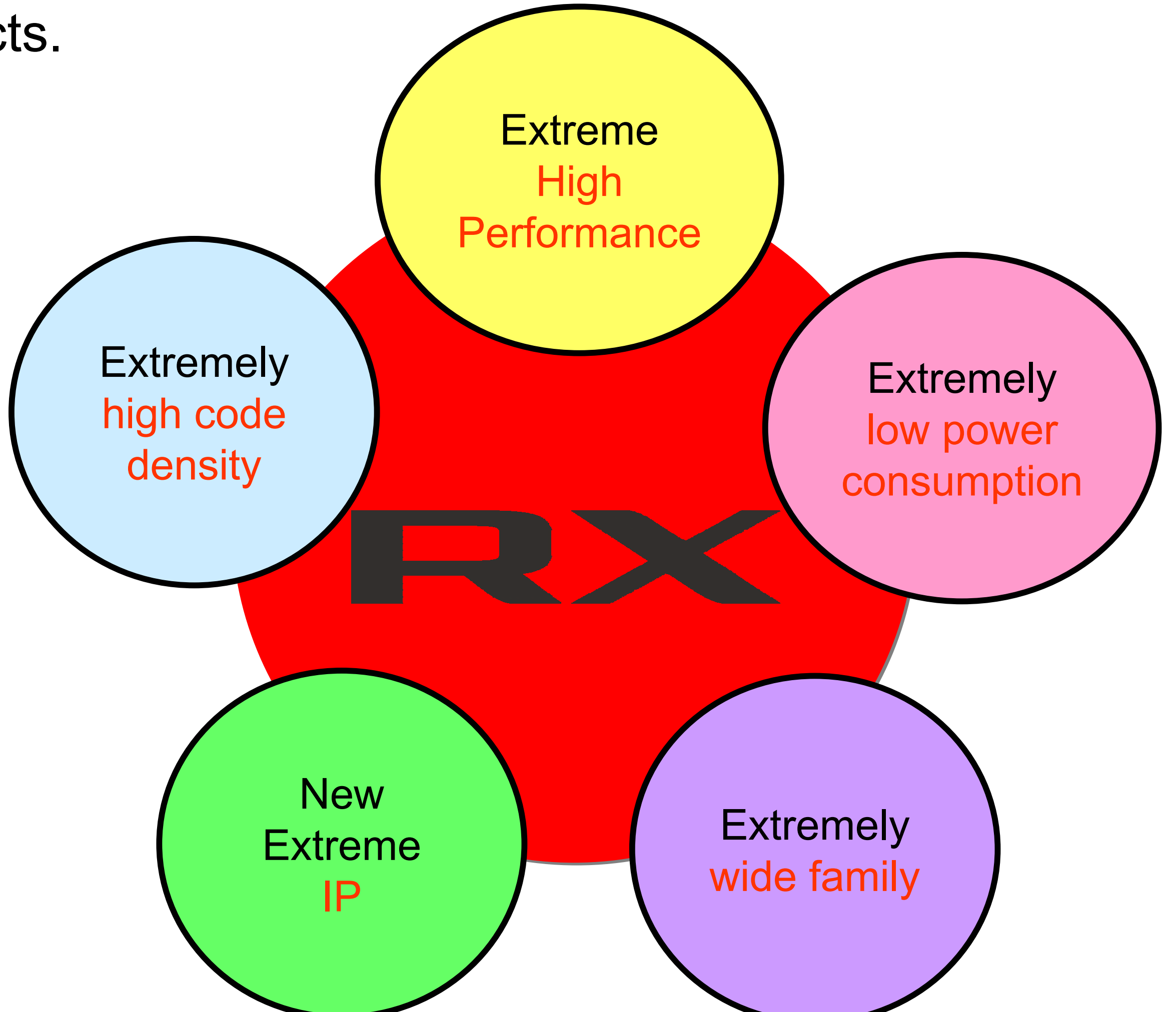
The RX Concept

- The RX aim is to realize higher maximum operating frequency, better performance, improved code efficiency, and lower power consumption than previous products.



Compare to Competitors (Data from Web)

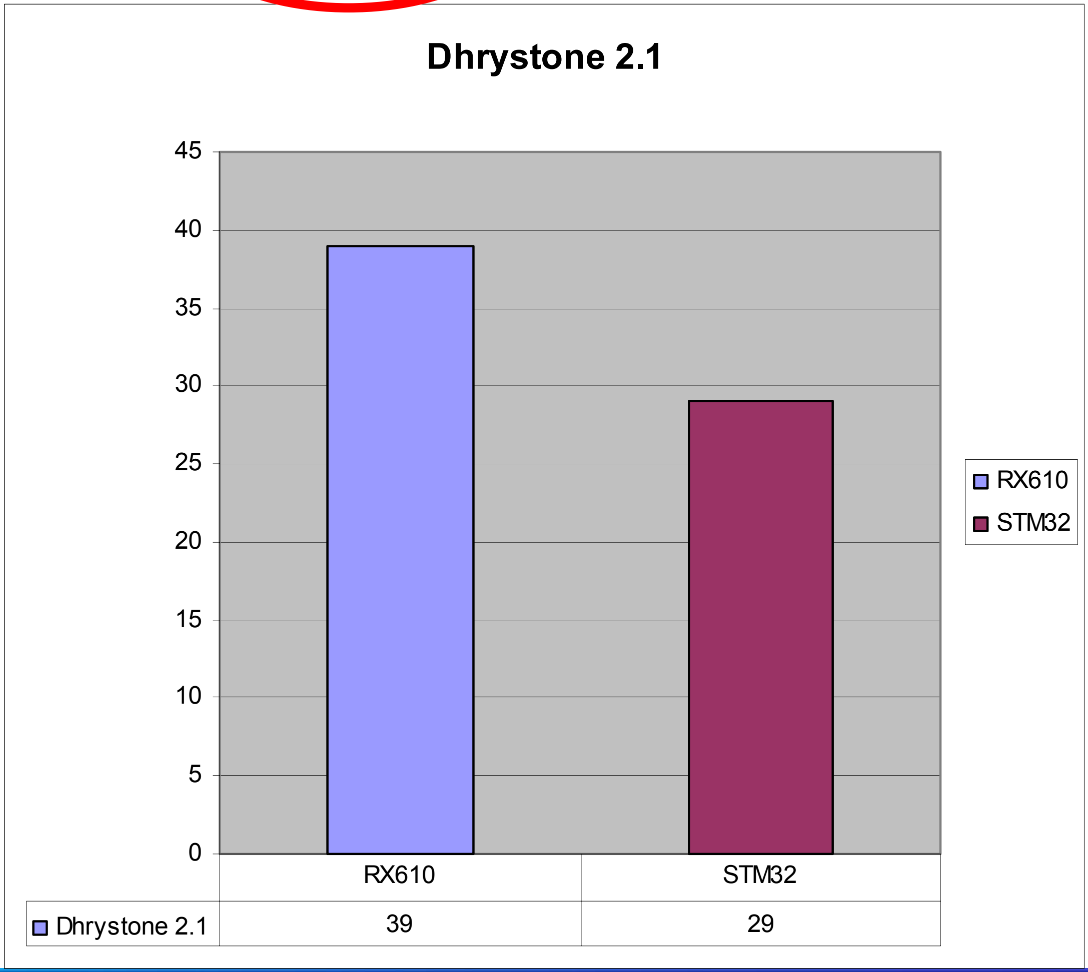
- Compared to the competitors, RX achieves 1.65DMIPS/MHz w/Dhrystone.

MIPS	→	1.5 DMIPS/MHz
AVR32 UC3	→	1.3 DMIPS/MHz
STM32 (Cortex M3)	→	1.25 DMIPS/MHz
ARM 9	→	1.04 DMIPS/MHz
ARM 7	→	0.95 DMIPS/MHz
ColdFire V2	→	0.94 DMIPS/MHz(SRAM)
ColdFire V2	→	0.76 DMIPS/MHz (Flash)

RX
1.65
DMIPS/MHz

Dhrystone 2.1

- CPU:
  - RX610: 24 MHz (Single Cycle, 0 Wait State Flash Memory Access)
  - STM32: 24 MHz (Single Cycle, 0 Wait State Flash Memory Access)

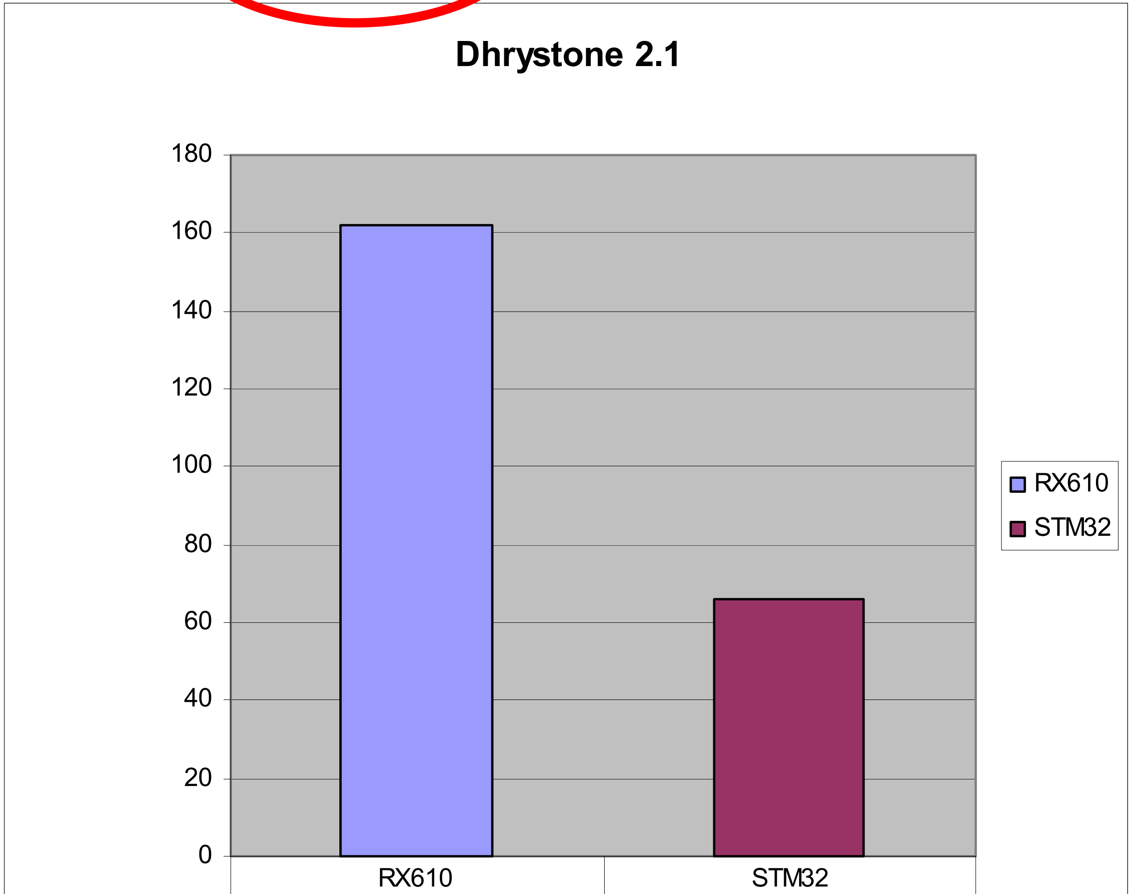


Result:

STM32 offers lower performance at same frequency than RX

Dhrystone 2.1

- CPU:
  - RX610: 100 MHz (Single Cycle, 0 Wait State Flash Memory Access)
  - STM32: 72 MHz (Multi State Flash Memory Access)



	RX610	STM32
Dhrystone 2.1	162	66

Result:

STM32 offers only

0.9 DMIPS/MHz

@ 72MHz

What's Unique about RX600?

- **RX600 is the only Flash CISC MCU with zero-wait-state Flash at full speed**
  - Truly **165 DMIPS** at 100MHz operation
  - Deterministic operation

- **Hardware Floating Point Unit (FPU) and 1-cycle Multiply Accumulate (MAC)**
  - FPU for fast, simple, compact math
  - FPU, DSP functions, and fast ADC complement the Integrated Motor Control timer
  - Harvard Architecture further improves DSP performance

- **Low Power Consumption**
  - **500uA/MHz** with all peripherals on, linear consumption
  - **0.9 uA** Deep Standby

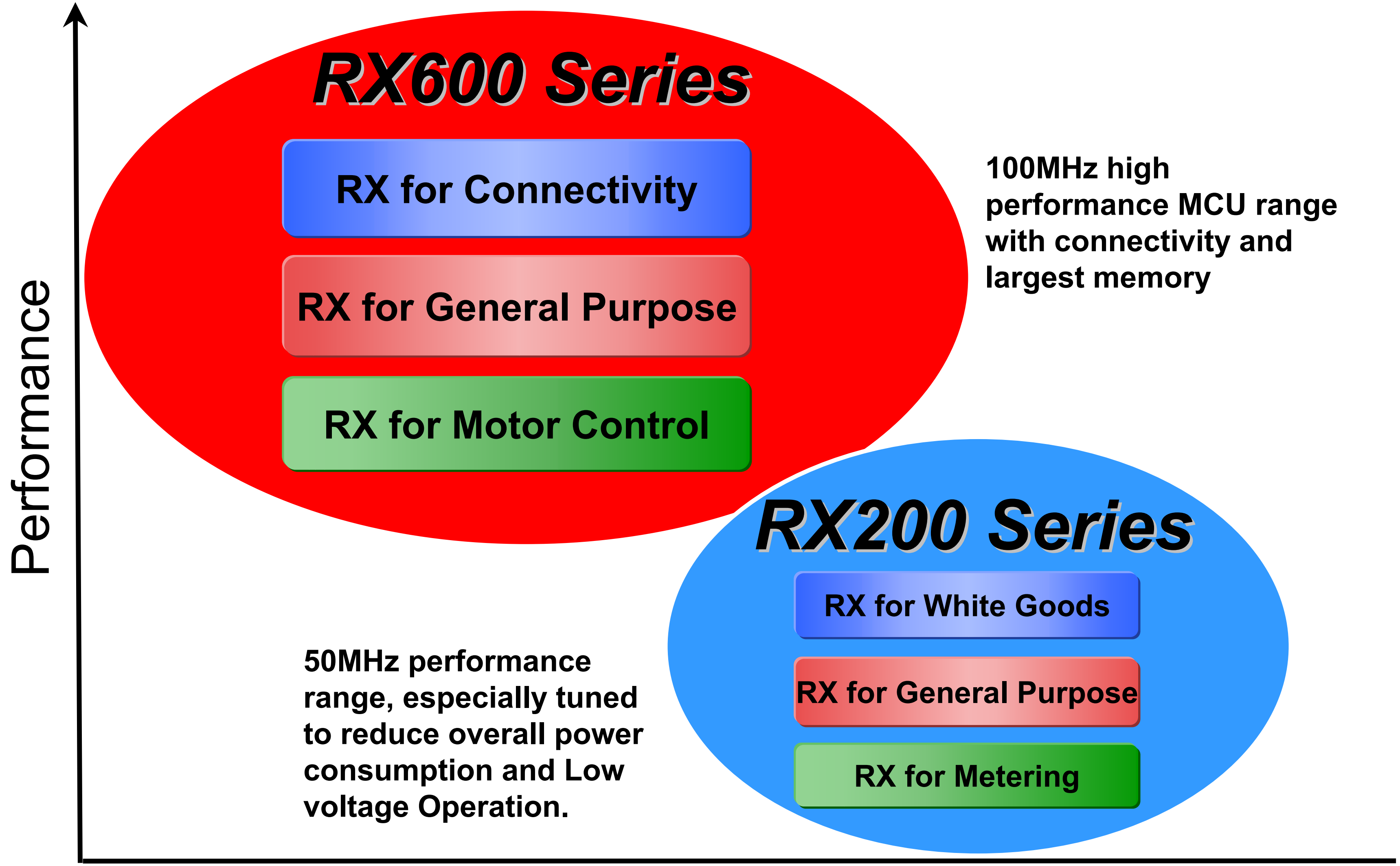
- **Embedded 32KB data flash (30k to 100K erase and write cycles)**

- **Most compact code size**
  - More compact than leading 32-bit cores in Flash MCUs

- **Flash MCU with up to 1 USB host or 2 USB Device, Ethernet and CAN interfaces**

RX Platform Overview

- Renesas extreme Microcontroller RX platform comes in two Series.



RX600 family road map

RENESAS RX

RX610
768k-2MB Flash
128k RAM
144, 176pin

RX62N
384k-512kB Flash
64k-96k RAM
85, 100, 144, 176pin
USB (Host/Device/OTG)
CAN (0ch or 1ch)
Ethernet MAC

RX621
256k-512kB Flash
64k-96k RAM
85, 100, 144, 176pin
USB (Host/Device/OTG)
CAN (0ch or 1ch)

RX62T
64k-256kB Flash
8k-16k RAM
64, 80, 100, 112pin
Two Motor Timer units
12bit ADC
3 integrated Op Amps

RX6xx
Enhanced memory & package lineup
Reinforcing peripheral functions

Connectivity

RX6xx
Enhanced memory & package lineup
Reinforcing peripheral functions

RX6xx
Enhanced memory & package lineup
Reinforcing peripheral functions

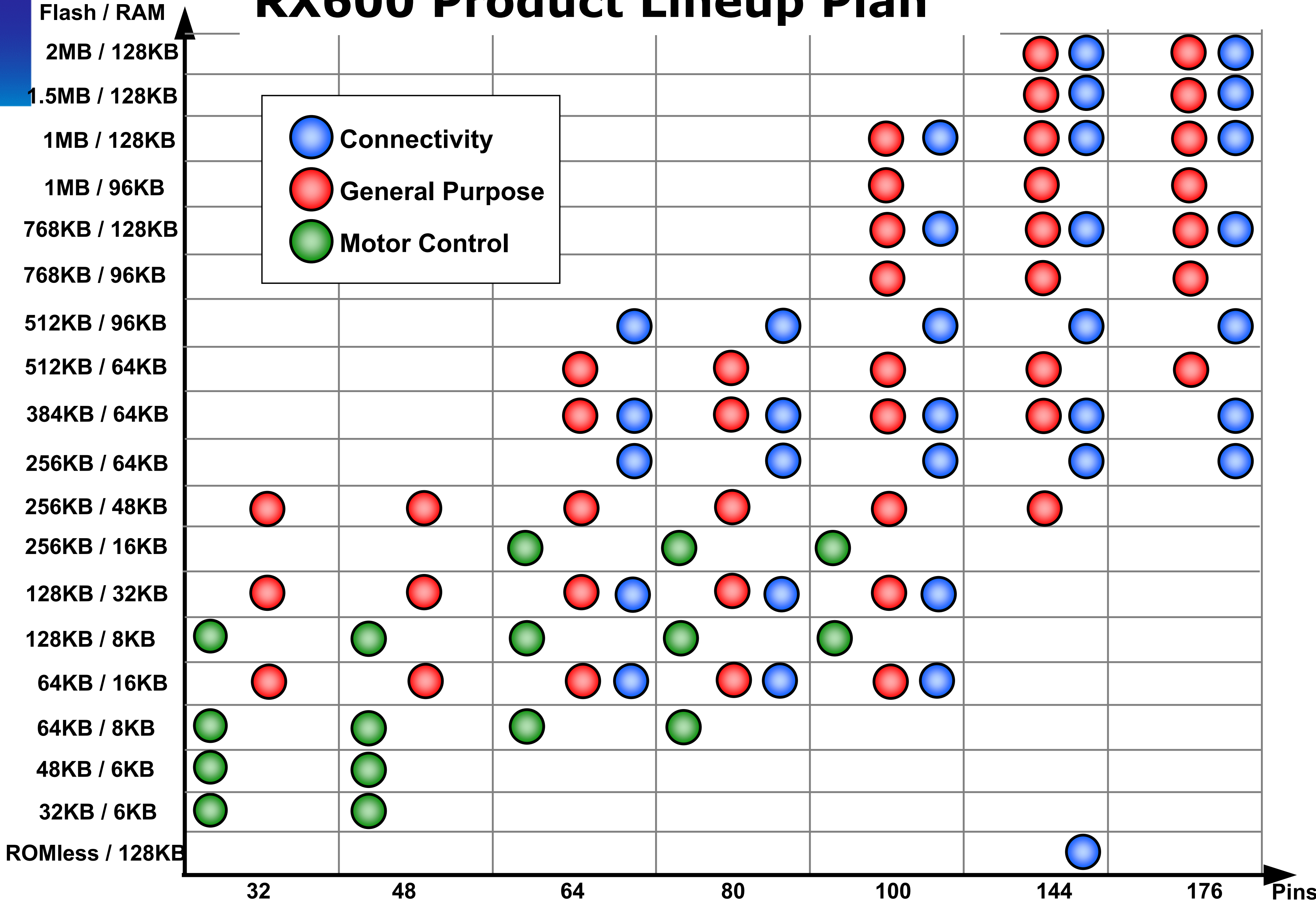
General Purpose

RX6xx
Enhanced memory & package lineup
Reinforcing peripheral functions

Motor Control

2009 **2010** **2011**

RX600 Product Lineup Plan



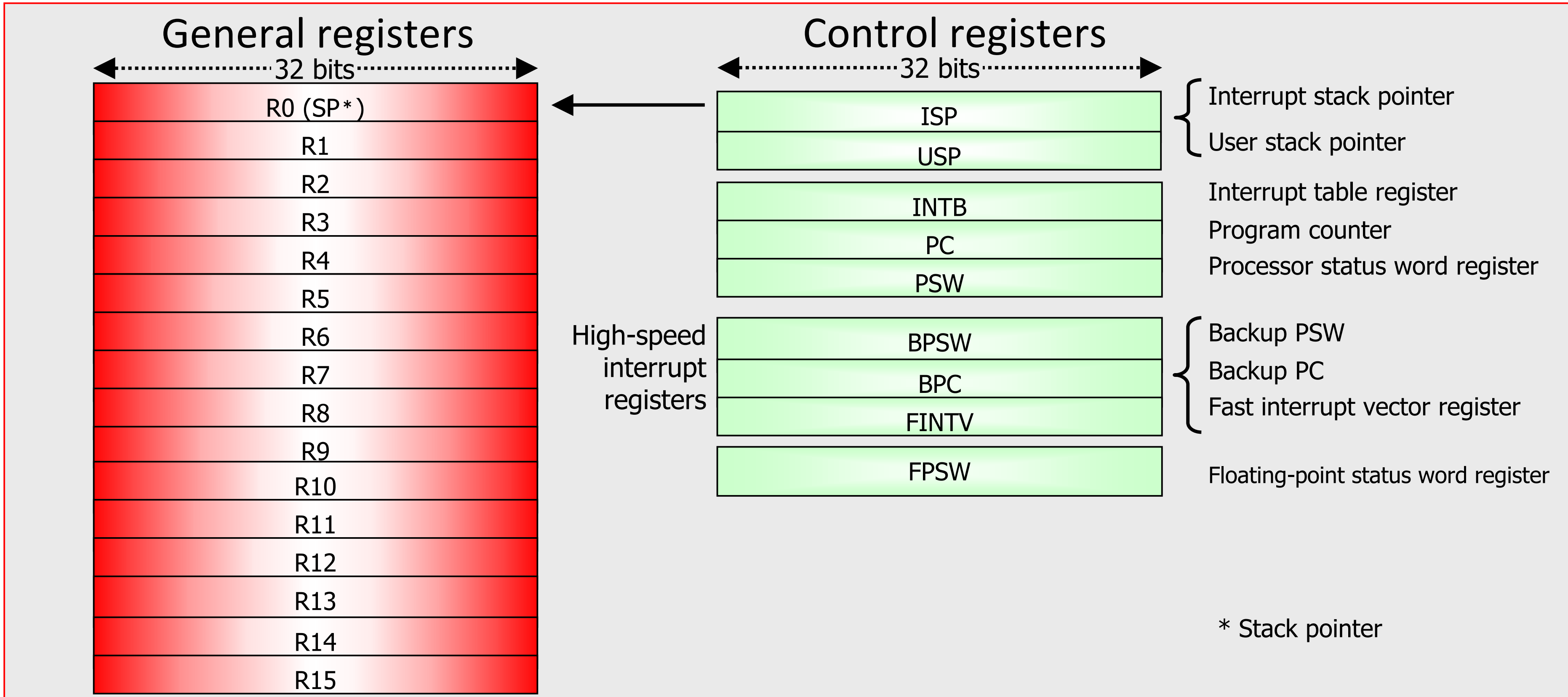
RX600 basics and features

RX CPU – The Basics

Item	Specification
CPU	Harvard Architecture
	Variable length instruction format (1 to 8 Bytes)
General Registers	16 x 32-bit
Instructions	73 9 DSP 9 FPU
Endian mode	Instructions: little-endian Data: big and little-endian
Address space	4GB linear
Addressing modes	10
Floating point arithmetic unit	Single precision (32-bit)
Memory protection unit	Optional component
Operation frequency	Up to 200MHz
Performance	1.65MIPS/MHz

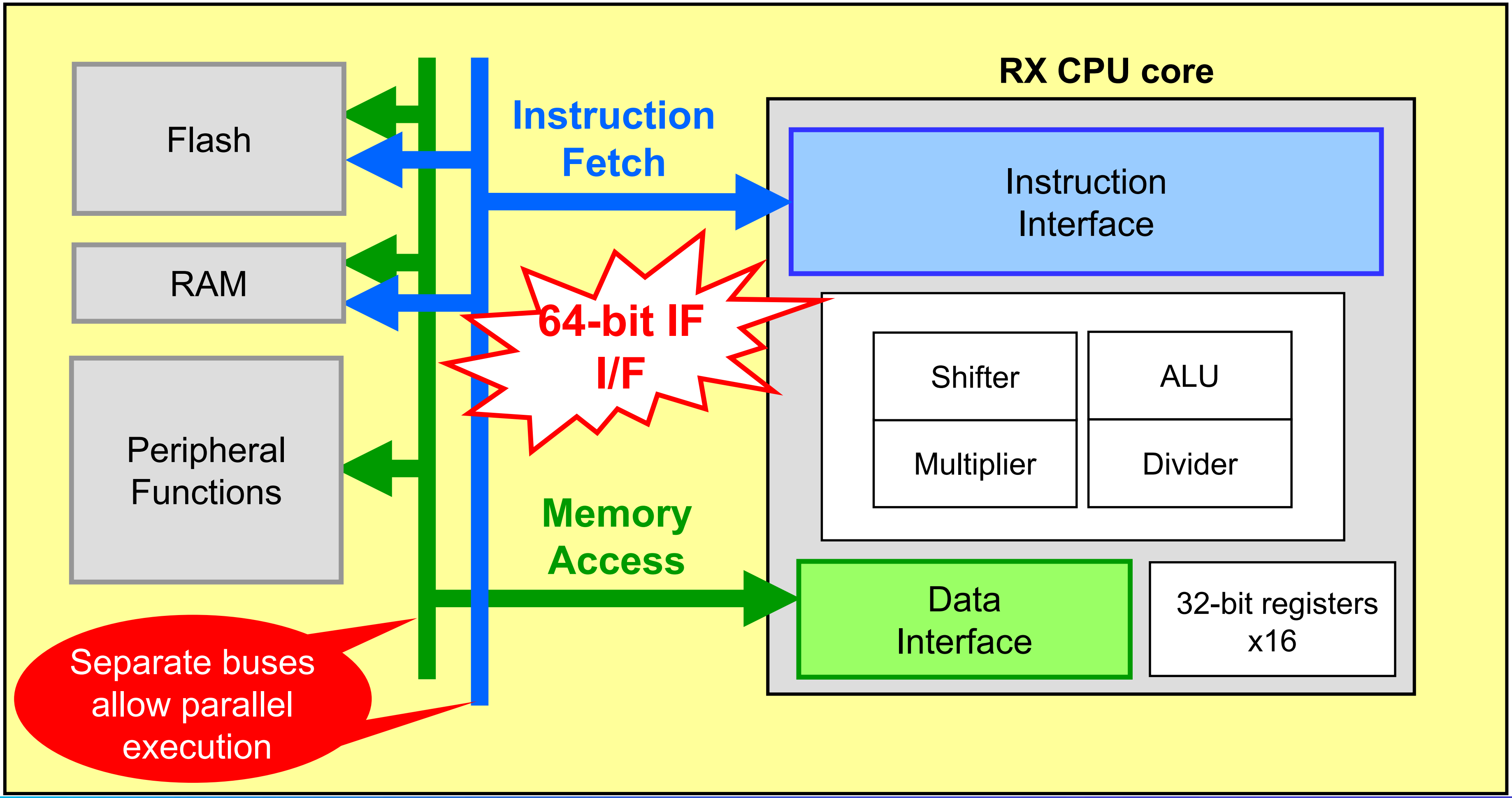
RX 32bit CPU

- 16 General 32-bit Registers speeds execution and reduces code size
- Use of General Registers simplifies compiler optimization
- Register-Register operations reduce memory accesses
- Dedicated High-speed Interrupt Control Registers
- General Registers can be allocated for Interrupt use as well



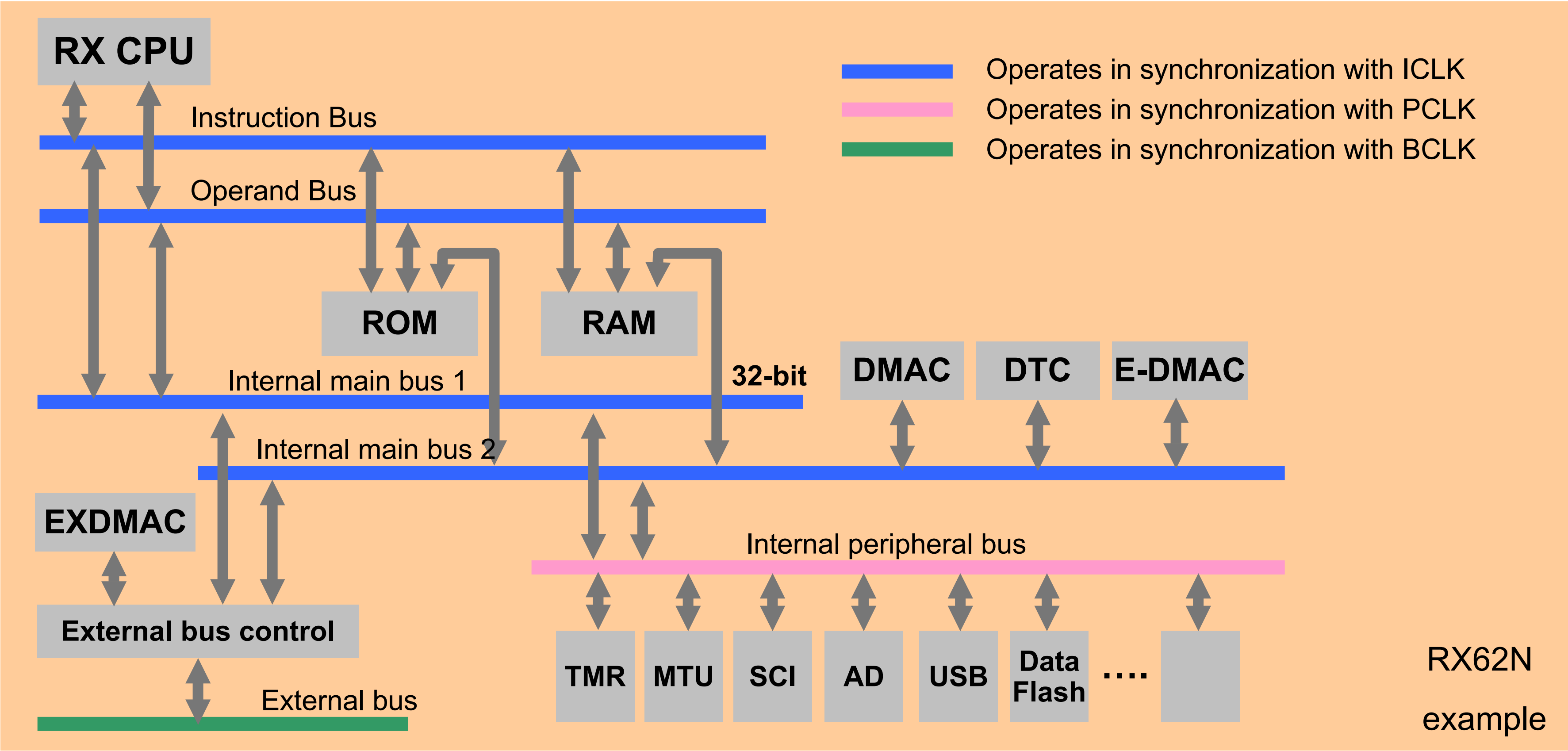
Enhanced Harvard Architecture

- Simultaneous execution of instruction fetches and memory accesses boosts pipeline performance and combined memory mapping keeps flexibility



RX600 internal bus configuration

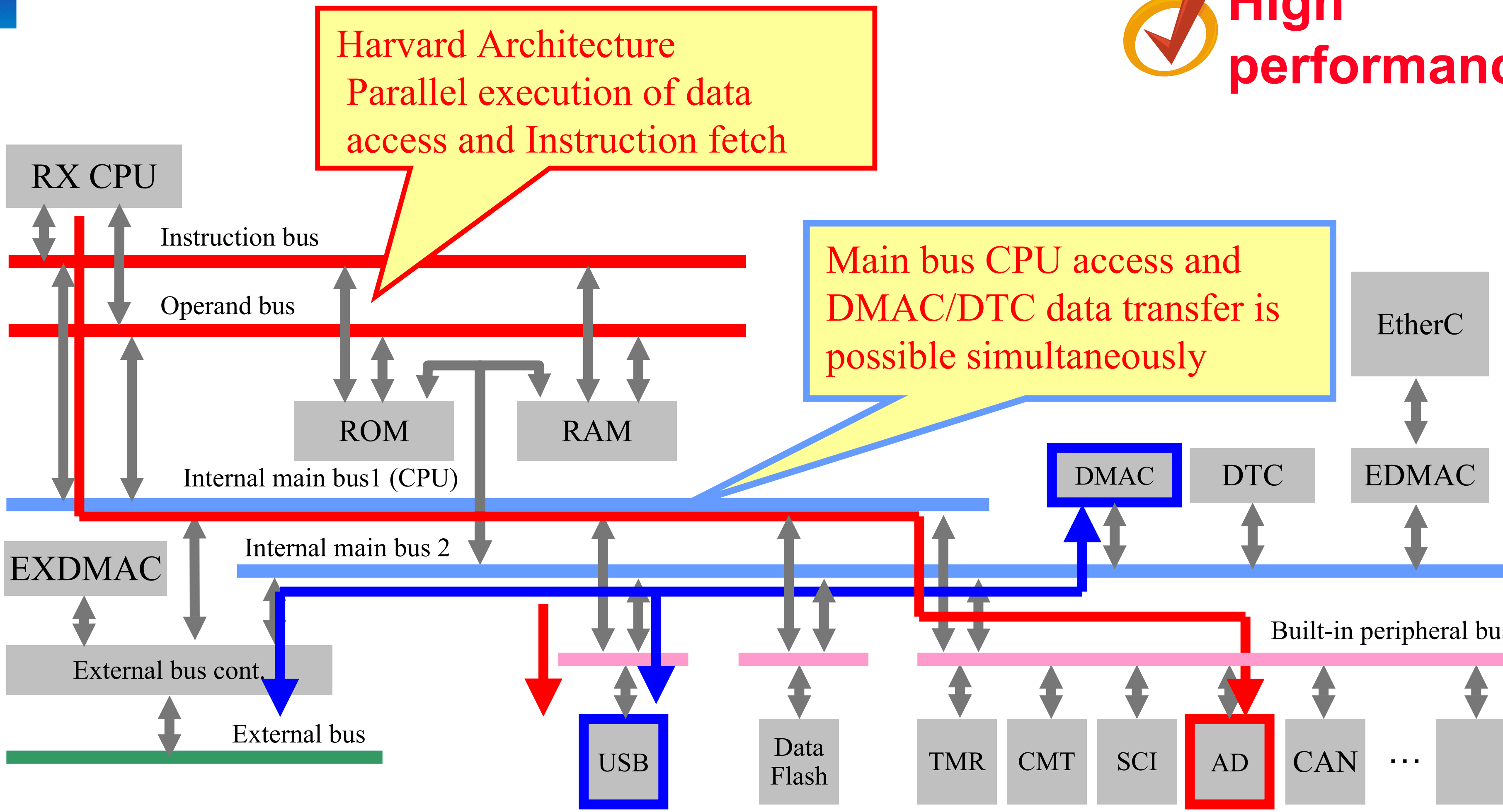
- RX600 includes up to 5 internal busses to enhanced data processing and to secure that there is no bottleneck between the CPU, Memory, DMA, peripherals and external bus.
- 2 dedicated CPU busses: instruction and operand
- 3 other main internal busses: simultaneous transfer of data from multiple masters



RENESAS

RX Family Internal bus structure

High performance



- RX600 includes up to 5 internal busses to enhanced data processing and to secure that there is no bottleneck between the CPU, Memory, DMA, peripherals and external bus.

RX Pipeline

- The RX CPU has a 5 stage Pipeline.

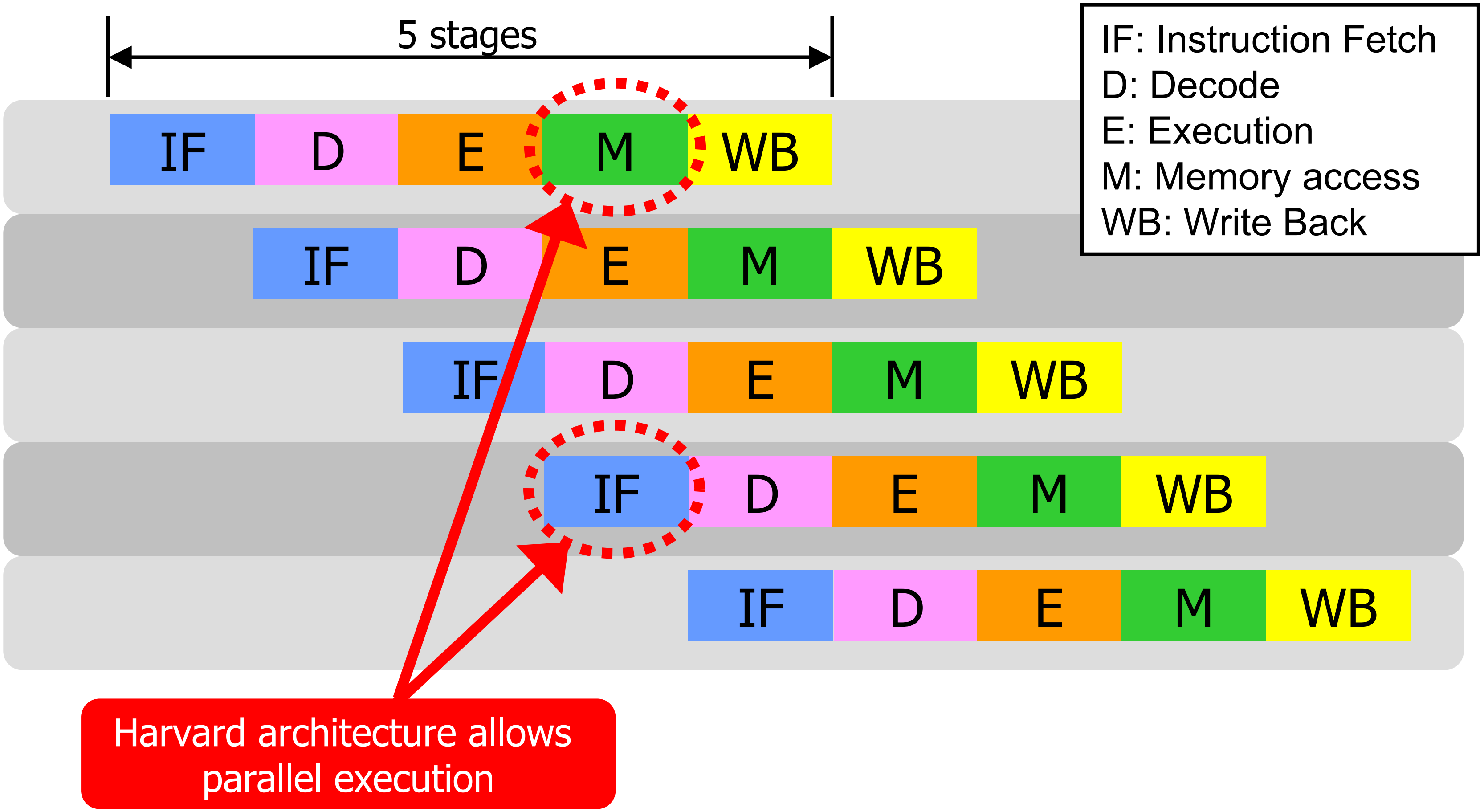
- CPU instructions (1 to 8 bytes in length) are converted into one or more micro operations.
- These micro operations are then executed by pipeline processing.

- The IF stage is executed in the unit of instructions.
- The D (and following) stages are executed in unit of micro operations.
- The CPU decodes the instructions in the D stage and converts them in micro-operations.

- The CPU has four 8-byte instruction queues.
  - It fetches until the instruction queue is full, regardless of the completion of the decoding stage.
  - As the Instruction bus is 64-bits, a single clock cycle will fetch 8 bytes.
  - A minimum of 1 instructions, a maximum of 8

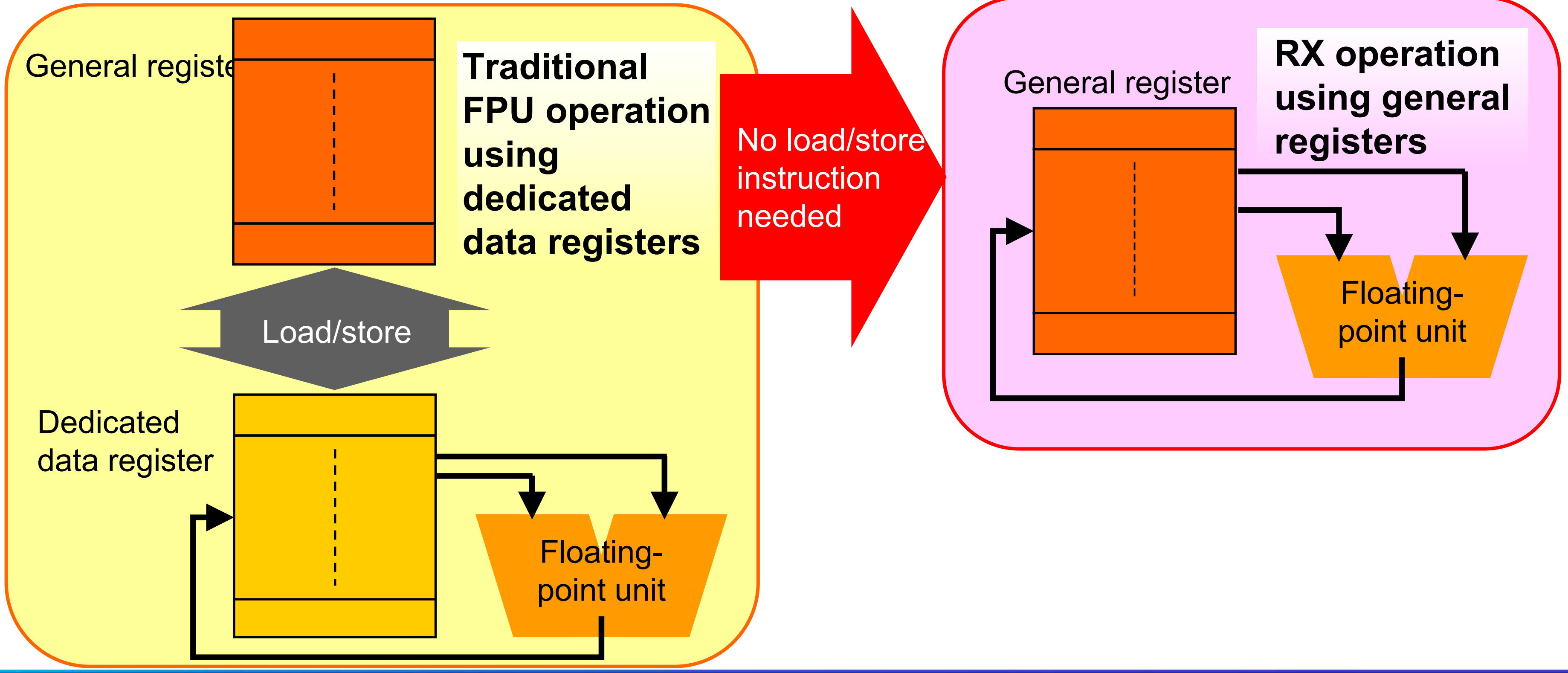
Five Stage Pipeline

- Parallel execution of instruction fetch and data memory access provides ideal execution rate of one clock cycle per instruction.



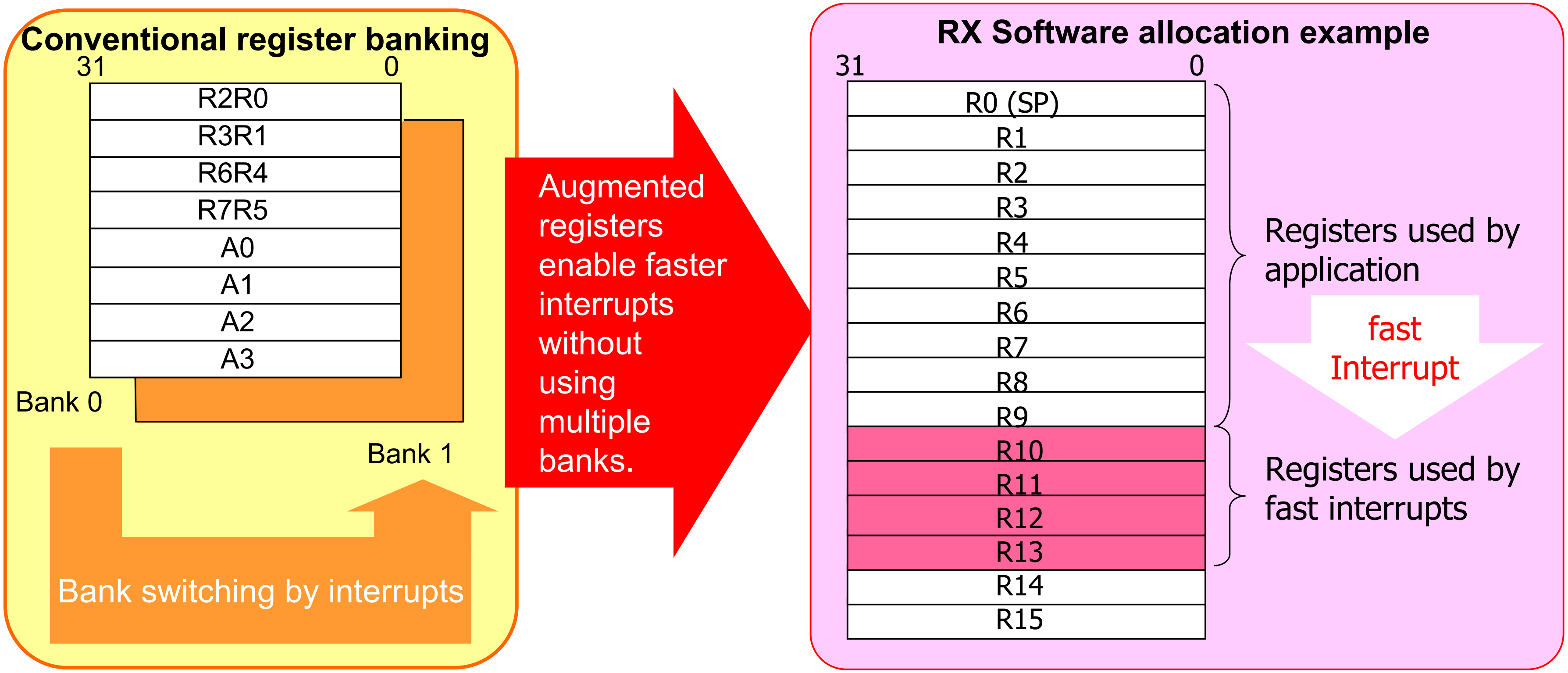
Single-Precision Floating-Point Unit

- The single-precision (32-bit) data format defined in IEEE 754* is supported.
- The exceptions defined in IEEE 754 are supported.
- Subtract, multiply, divide, and integer-convert instructions general registers are supported.
- The benefit of this implementation, FPU operates using main CPU registers rather than with its own register set. This speeds overall performance making floating calculation to an easy task.



Faster Interrupts through Register Allocation

- Augmented general registers can be allocated for dedicated use by interrupts to **increase speed**.
- Program counter and Status Word will be automatically backup before interrupt execution.
- A number of registers can be allocated to handle application interrupts.
- So saving registers on stack by push/pop instruction is not required anymore.
- High-speed interrupt sequences and allocation of general registers boost performance by about 50%.



Fastest Interrupt Response

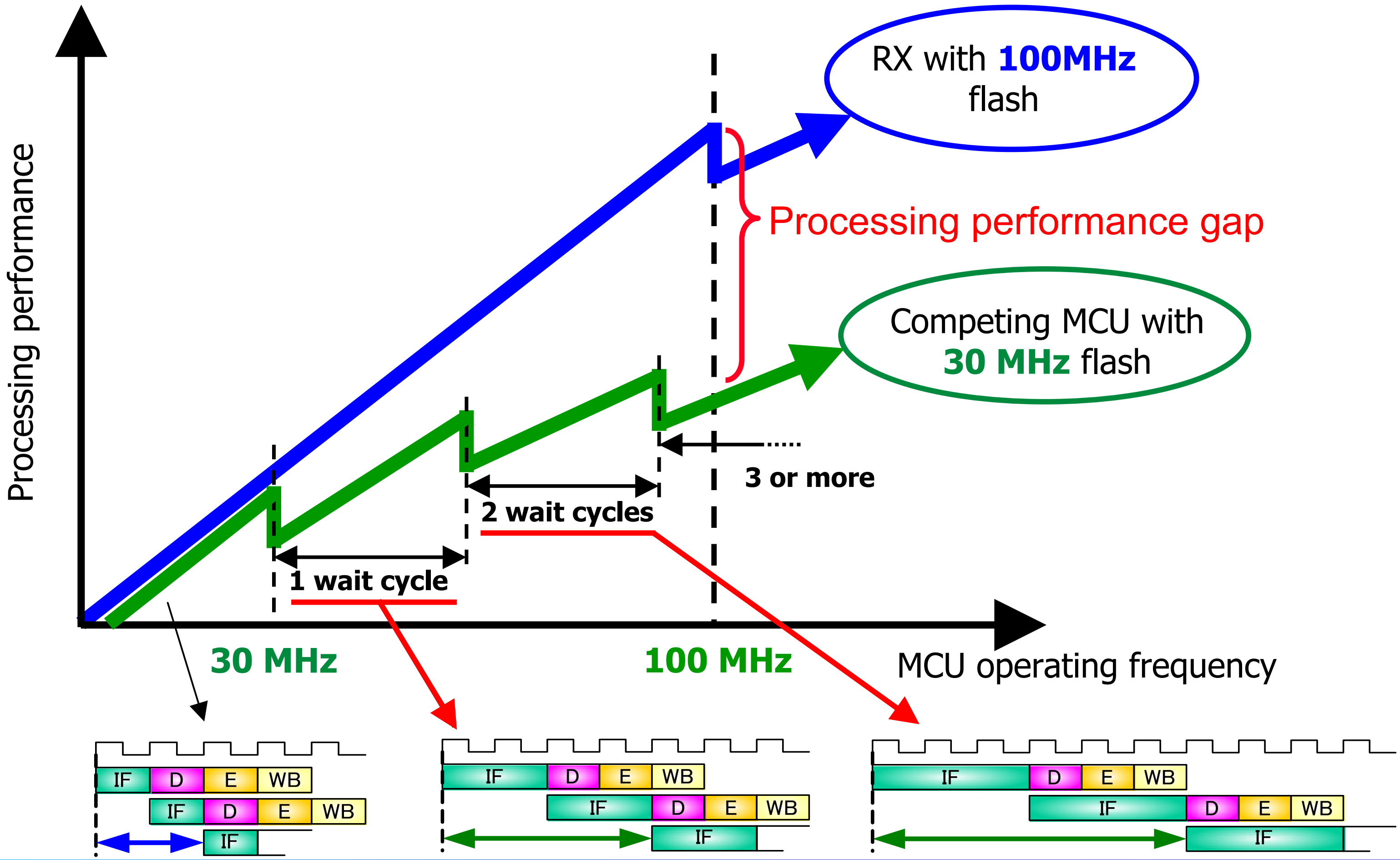
- Number of Cycle to the execution of first instruction in ISR

Architecture	Cycles (C Compiler)	Comment
RX600	5	Constant to CPU speed up to 100MHz
Cortex-M3	12	More when CPU freq > Flash speed
ARM7TDMI	24 – 42	More when CPU freq > Flash speed
MIPS M4K (PIC32)	18 – 40+	More when CPU freq > 30 MHz

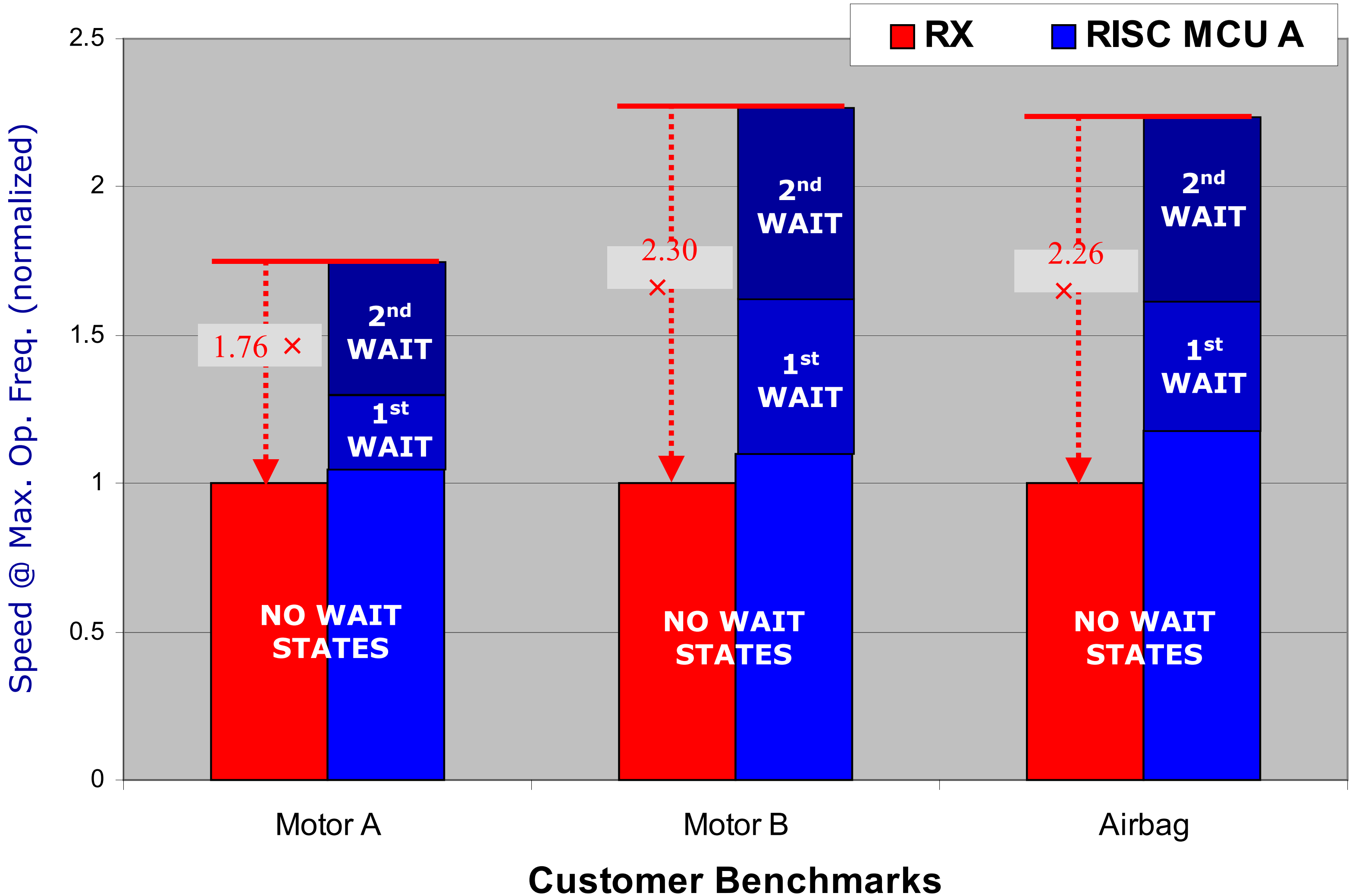
Sources:
1. Cortex-M3, ARM7TDMI: An Introduction to ARM Cortex-M3 Processor. http://www.arm.com/pdfs/IntroToCortex-M3.pdf
2. Estimated based on flash frequency, dedicated register bank, register size and C32 compiler code generation

RX Flash Performance=MCU Performance

- Maximum operating frequency and overall processing speed
- Access speeds up to 100 MHz with no wait cycles
- This saves time any and power consumption as equivalent level of CPU performance could be reached at lower frequency.



True Performance



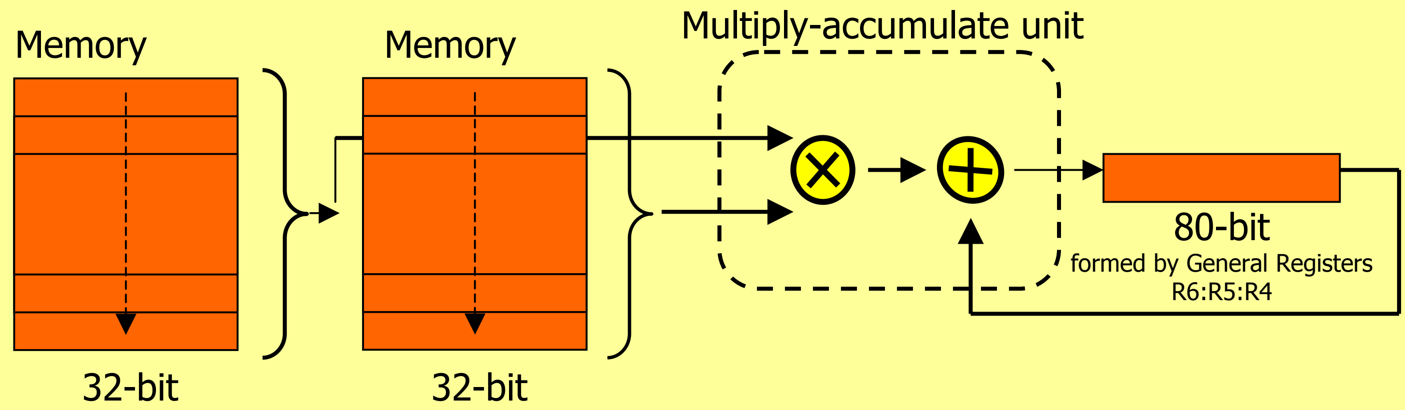
- Approximately 2x faster than best in class RISC!

Benchmarking disclaimer: Your results may vary*

DSP Arithmetic Functions

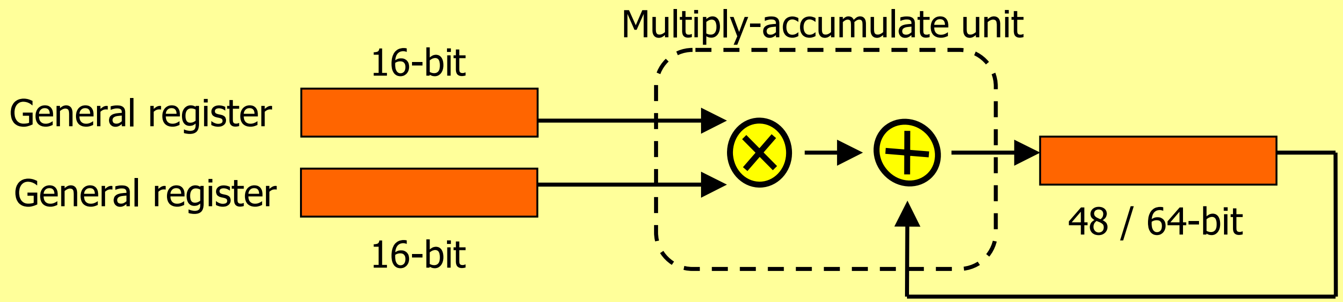
- The memory-to-memory multiply-accumulate operation instruction (RMPA) is ideal for sequential multiply-accumulate operations on accumulated data, resulting in more precise 32-bit arithmetic operations.
- Instruction RMPA can easily be accessed on C-level with compiler instrinsic functions.
- RMPA can be interrupted to avoid delay of interrupt acceptance.

Memory-to-memory multiply-accumulate operation instruction (RMPA)

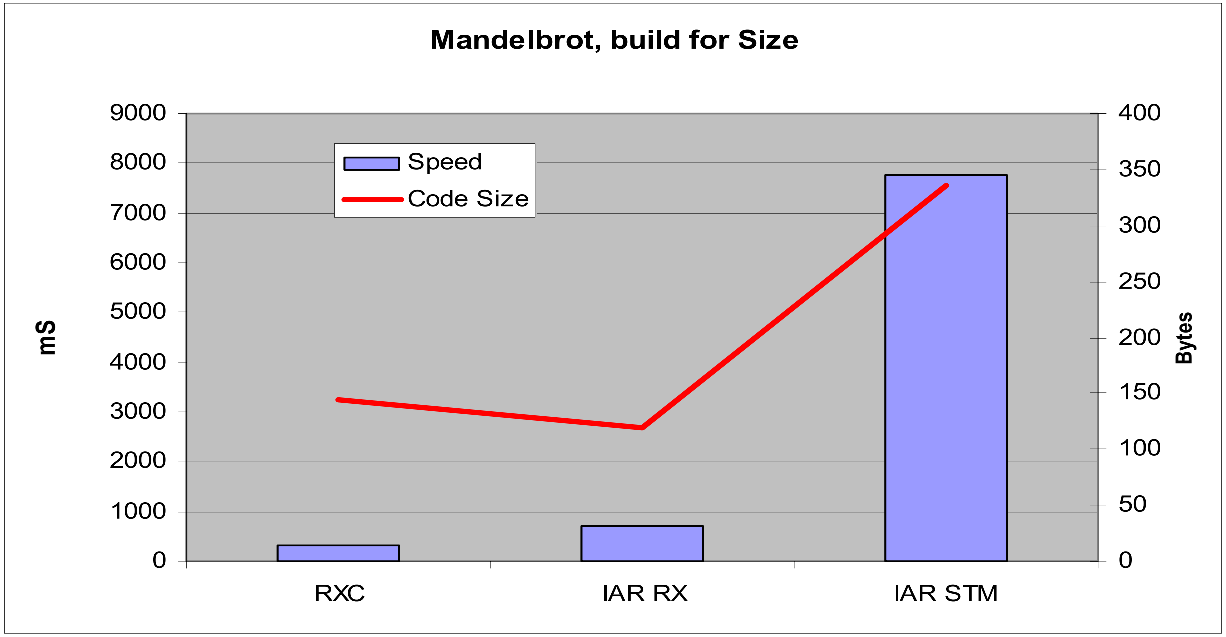


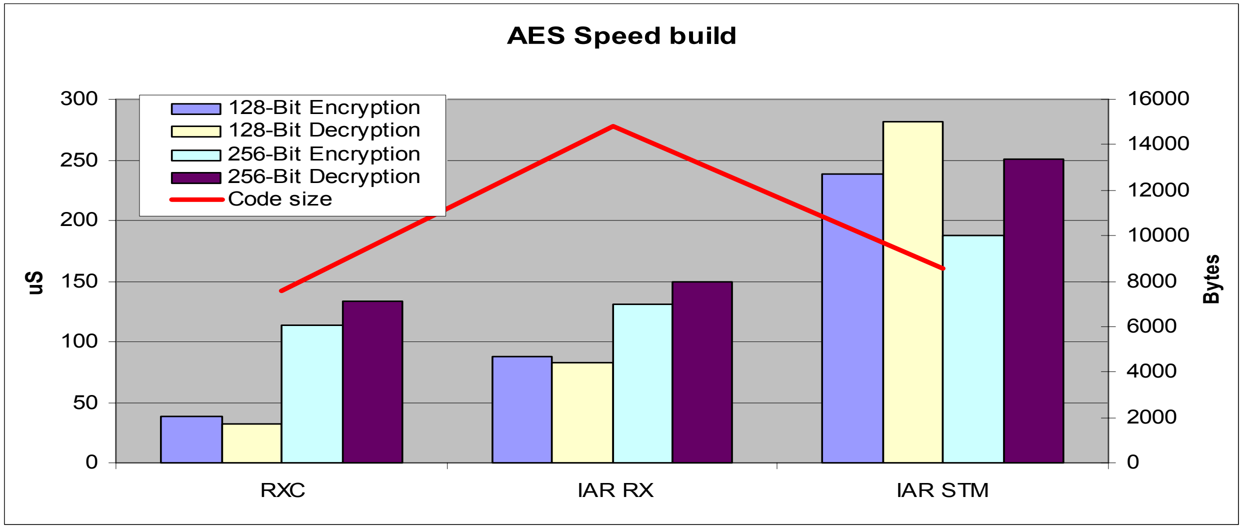
- The register-to-register multiply-accumulate operation instruction (MAC) eliminates the need for data transfer from general registers to memory, resulting in high-speed operation.

Register-to-register multiply-accumulate operation instruction (MAC)



DSP functions



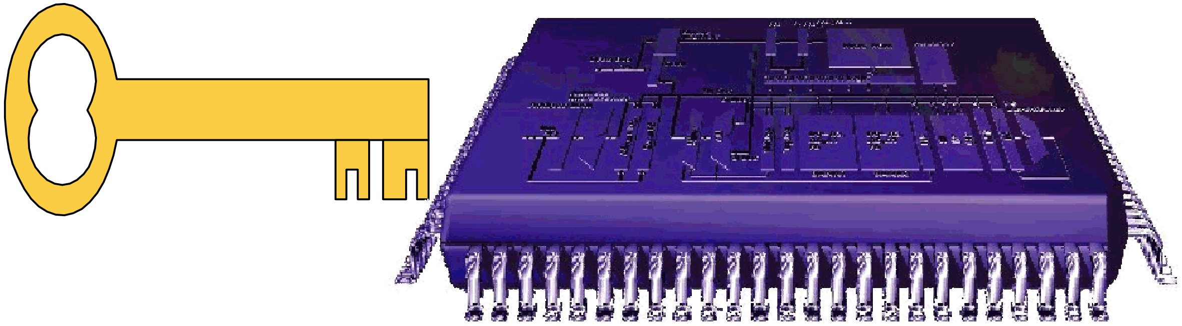


FLASH Security

- Security of the Flash memory is controlled by an ID code.
  - A code is used to secure the Flash in Boot and On-Chip Debug Mode.
    - 16 bytes (1 Control Byte, 15 ID bytes = 120 ID bit)

	31 24	23 16	15 8	7 0
FFFF FFA0h	Control code	ID code 1	ID code 2	ID code 3
FFFF FFA4h	ID code 4	ID code 5	ID code 6	ID code 7
FFFF FFA8h	ID code 8	ID code 9	ID code 10	ID code 11
FFFF FFACh	ID code 12	ID code 13	ID code 14	ID code 15

- The use of the ID code, results in differing levels of security.
- This prevent read-out and erase according to the user needs making it secure.



FLASH Security – Boot Mode & OCD 1

- With in the Code Space, there is a 16 byte area.
  - If this area is populated with the code:

0x45,	0x01,	0x02,	0x03	0x45 is the Control Code
0x40,	0x41,	0x42,	0x43	All other bytes are 'User defined'
0x60,	0x61,	0x62,	0x63	
0x80,	0x81,	0x82,	0x83	

  - Then, the User has '3'attempts to connect to the device, specifying the correct code.
  - If an incorrect code is specified 3 times, the Flash will erase itself.

FLASH Security – Boot Mode & OCD 3

- With in the Code Space, there is a 16 byte area.
  - If this area is populated with the code:

0x52,	0x50,	0x72,	0x6f	0x52 is the Control Code
0x74,	0x65,	0x63,	0x74	This bytes are defined by
0xff,	0xff,	0xff,	0xff	Renesas.
0xff,	0xff,	0xff,	0xff	

  - Always judged to be a non-matching ID code.
  - Specify this code will erase the device at all connection attempts.

FLASH Security – Boot Mode & OCD 2

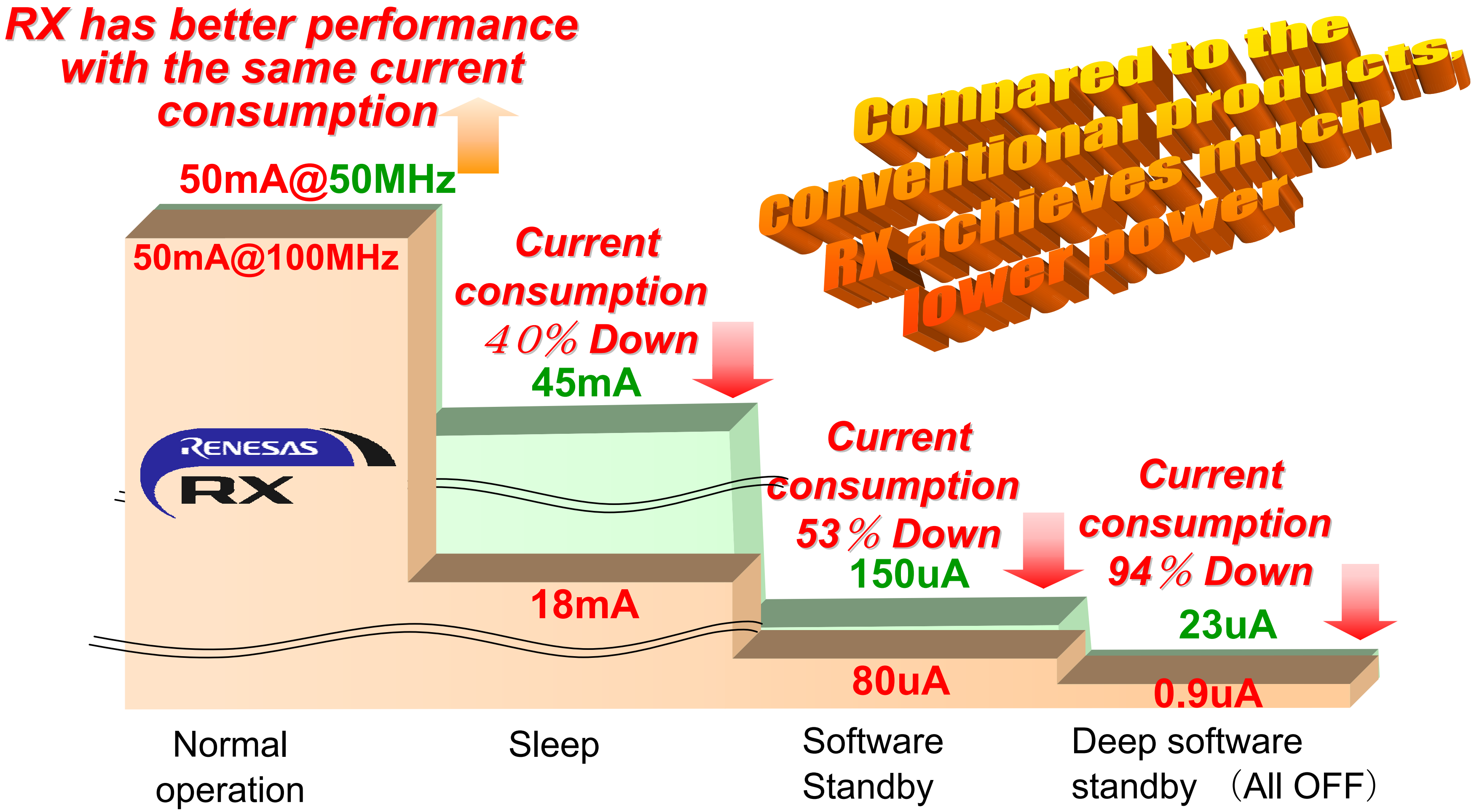
- With in the Code Space, there is a 16 byte area.
  - If this area is populated with the code:

0x52,	0x51,	0x73,	0x70	0x52 is the Control Code
0x75,	0x66,	0x64,	0x75	Bytes sequence other than that
0x01,	0x23,	0x45,	0x67	specified by Renesas.
0x89,	0xab,	0xcd,	0xef	See previous slide!

  - Then, the User to supply the correct code when connecting via Boot Mode and via OCD.
  - The Flash will erase itself if the ID code is wrong.
  - With 2^{120} code options, that is 1329227995784915872903807060280300000 options
  - it will have to be a good guess to get in.

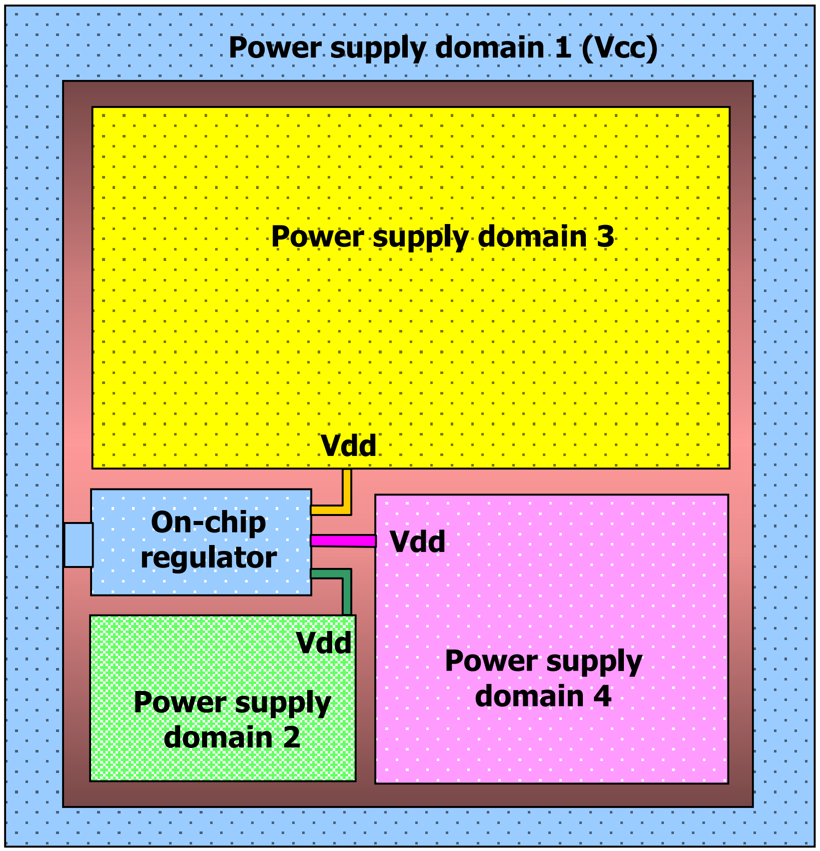
RX - flexible low current consumption

- RX supports selection of low power modes to reduce overall consumption.



Reduced Power Consumption: Power Domains

- Multiple power domain design methodology



Single Voltage Supply concept!

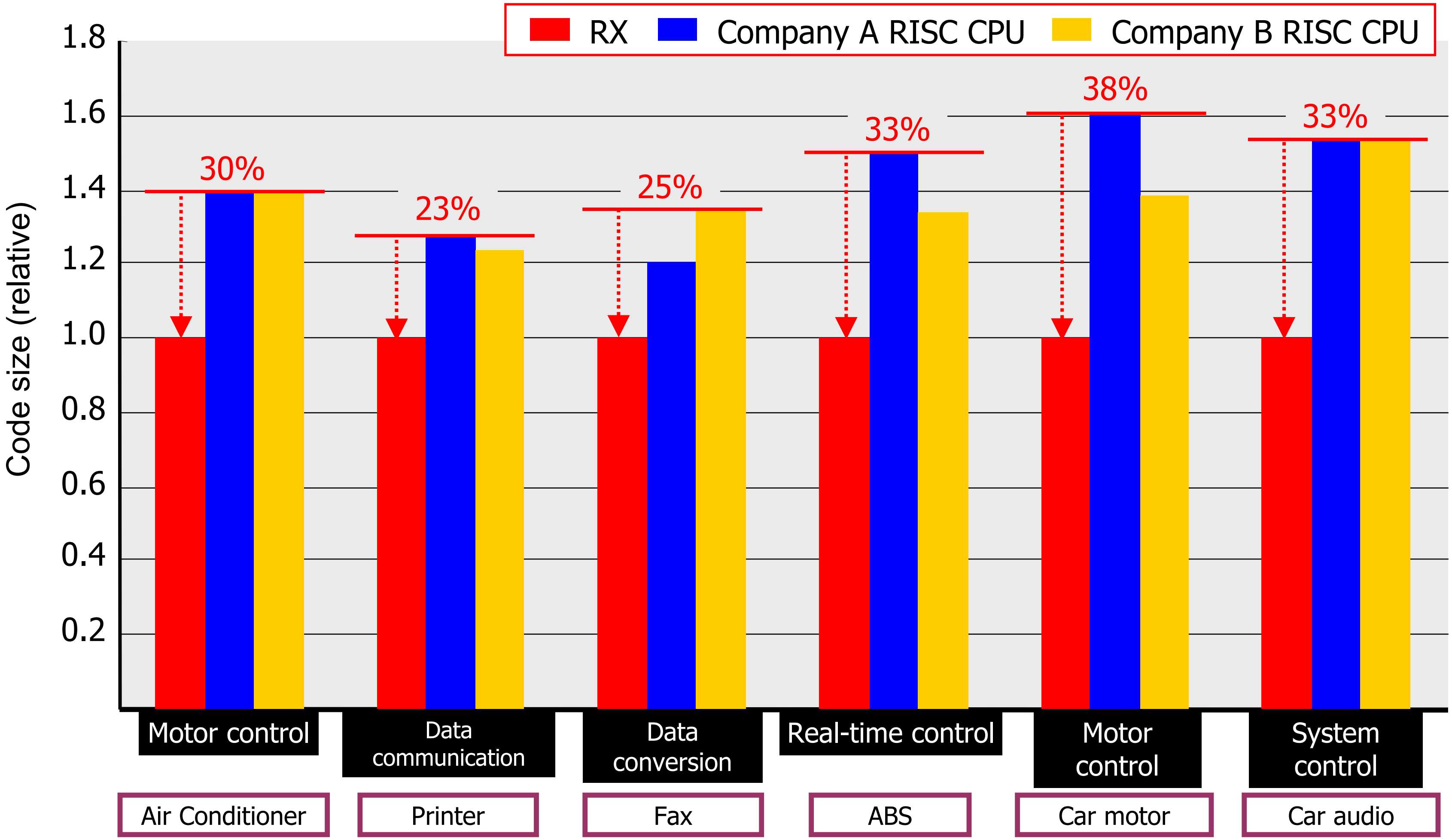
RX600: 500uA/MHz (full active)

	Domain 1	Domain 2	Domain 3	Domain 4
Normal operation	○	○	○	○
Power-down mode 1	○	○	○	×
Power-down mode 2	○	○	×	×
Power-down mode 3	○	×	×	×

RX600: 0.9uA (Deep Standby)

○ : Active block × : Inactive block

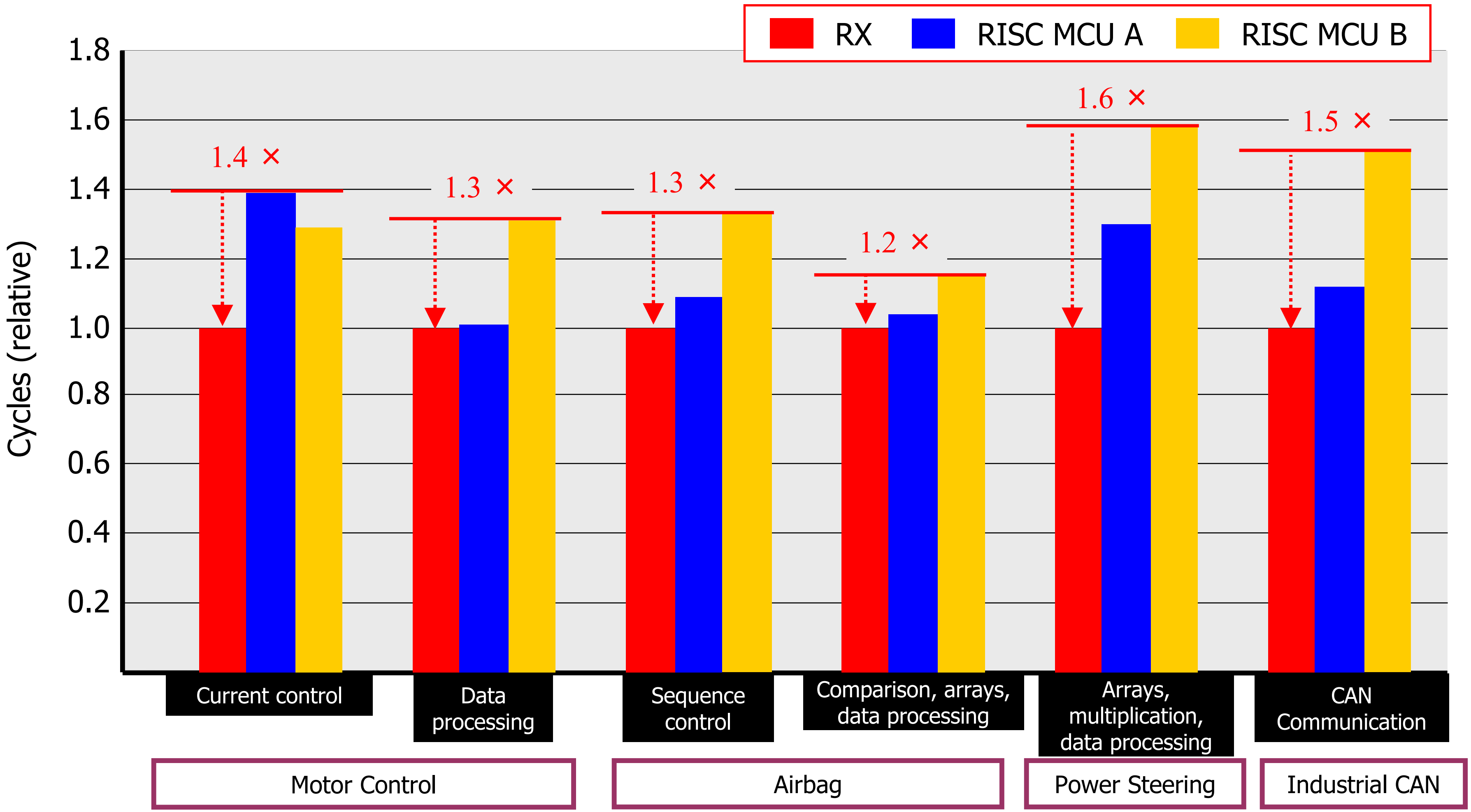
Code Size: RX vs. Competitors



- RX demonstrates superior code efficiency over competitors.

Benchmarking disclaimer: Your results may vary*

Cycle Count: RX vs. Competitors

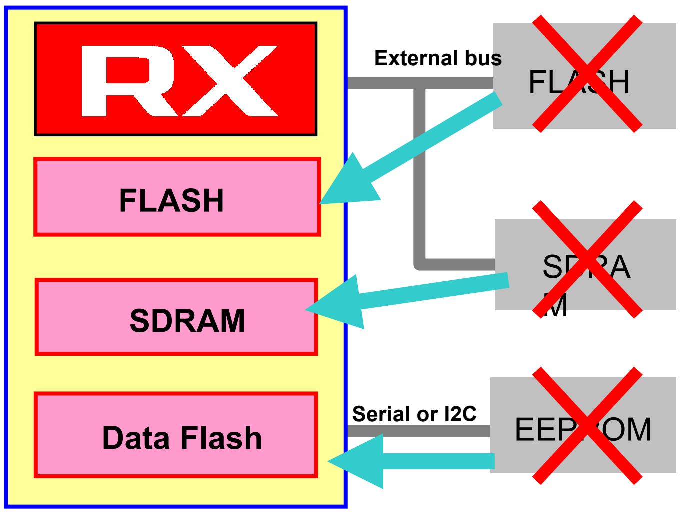


- RX achieves superior performance in cycle count.
- Higher operating frequency high speed flash will realize additional significant performance improvements.

Benchmarking disclaimer: Your results may vary*

Low cost System BOM

- RX600 has up to 2MB flash memory for programming and flash memory for data storage ,
- as well as up to 128 KB SRAM. These on-chip memories provide various advantages.



Advantages of On-Chip Memories

- Reduction of the board area
  - Advantageous for the small systems such as digital consumer appliances.
- Improvement of the board design efficiency
  - Minimized wiring reduces the mistakes in board design and shorten the development period.
- Reduced Parts
  - In addition to the memories, other parts such as resistors or capacitors can be reduced.
- Reduction of EMI noise
  - Reduced external signals generate less noise.
- Security
  - Information leakage from the external bus can be prevented.
- Increasing the number of effective pins on MCU
  - The pins which used to be connected to external memories can be assigned for other IO.

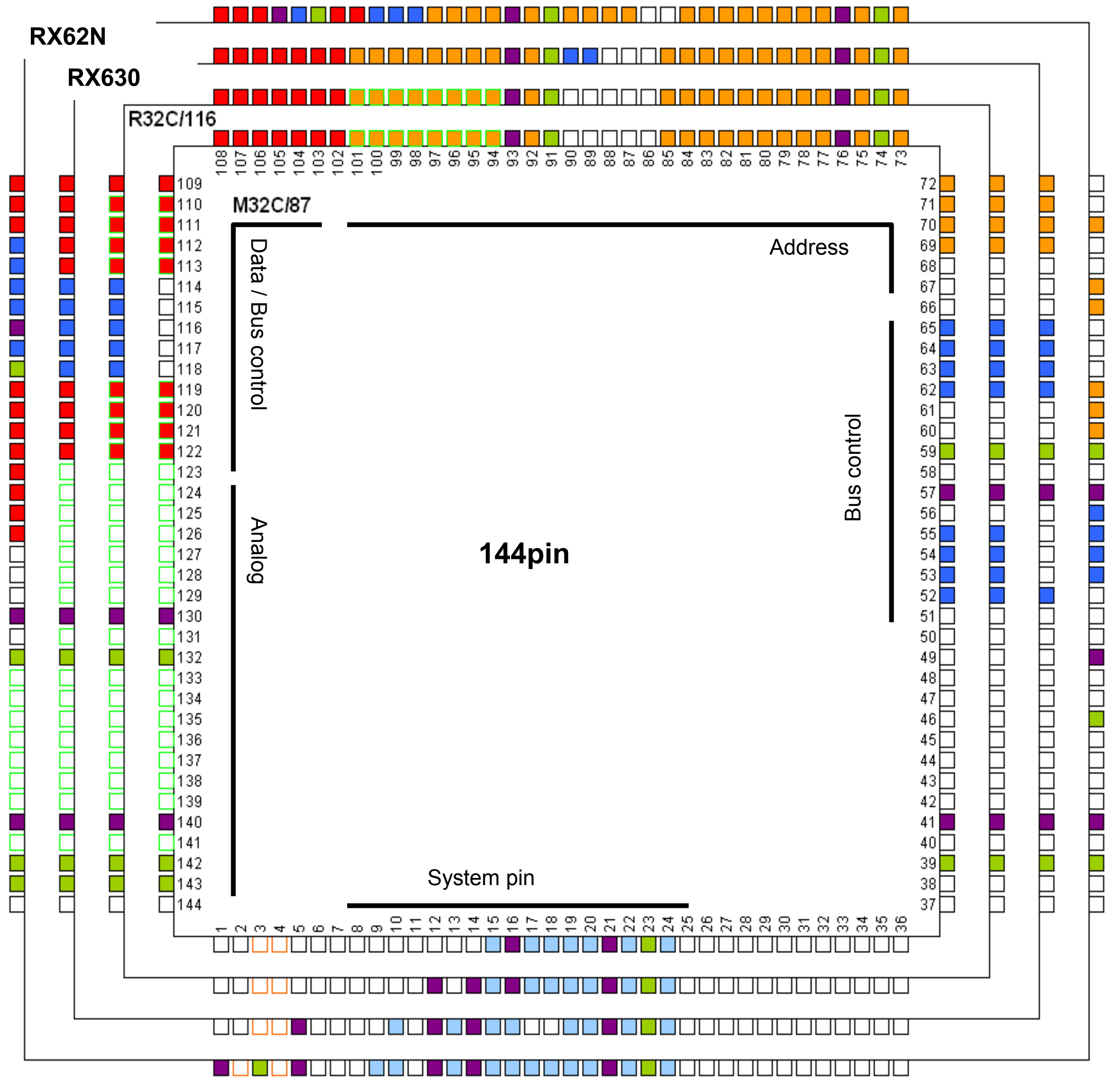
Flash Memory General Specification

RX610	Code-Flash	Data-Flash
P/E Temperature	Ta=-40～85 degC	
Read Temperature	Ta=-40～85 degC	
P/E Cycles	1,000	30,000
Data Retention	10year	10year
P/E Vcc	3.0v～3.6v	3.0v～3.6v
Read Vcc	3.0v～3.6v	3.0v～3.6v
Erase Time	50msec / 8kB (Typ.)	300msec / 8kB (Typ.)
Program Time	2msec / 256B (Typ.)	0.4msec / 8B (Typ.)

RX62N/RX621/RX62T	Code-Flash	Data-Flash
P/E Temperature	Ta=-40 ~ 85 degC	
Read Temperature	Ta=-40 ~ 85 degC	
P/E Cycles	1,000	30,000
Data Retention	10year	10year
P/E Vcc	2.7v～3.6v	2.7v～3.6v
Read Vcc	2.7v～3.6v	2.7v～3.6v
Erase Time	TBD sec / 4kB (Typ.) TBD sec / 16kB (Typ.)	300ms / 8kB (Typ.)
Program Time	TBD msec / 256B (Typ.)	0.4msec / 8B (Typ.)

Inheritance of the Pin Assignment – 144 Pin

- Inherits the pin assignment of R32C (RX610).
- While inheriting the basic pin assignment, the access speed to the external bus and other functions are improved. (RX62N)



- Data bus(D0-D15)
- Address bus
- Bus control signal
- System control pin
- Power supply (Vcc, AVcc, AVref etc.)
- Power supply (Vss, AVss, Vcl etc.)
- A/D input
- D/A output

RX610 Group

RX610 Group Features

RX610 Up to **2MB** Flash, high-speed performance **165DMIPS**, low power consumption **50mA@100MHz**,10bit **ADC 4ch x 4unit**

■ RX600 CPU

- ■ High-speed (100MHz), high performance (1.65MIPS/MHz) and low current consumption (50mA@100MHz)
- ■ Single-precision floating point unit FPU, barrel shifter, MAC, RMPA

■ Functions

- ■ 10bit ADC (1 μs conversion time) x 4 units each 4channel,
- ■ 10bit DAC 2 channel
- ■ up to 2MB single cycle access time flash memory
- ■ Large embedded 128KB RAM
- ■ Extreme number of communication functions (SCI: 7 ch, I²C for the fast mode Plus (1 Mbps))
- ■ Large number of timer functions (16-bit timer x 16 ch, 8-bit timer x 4 ch)

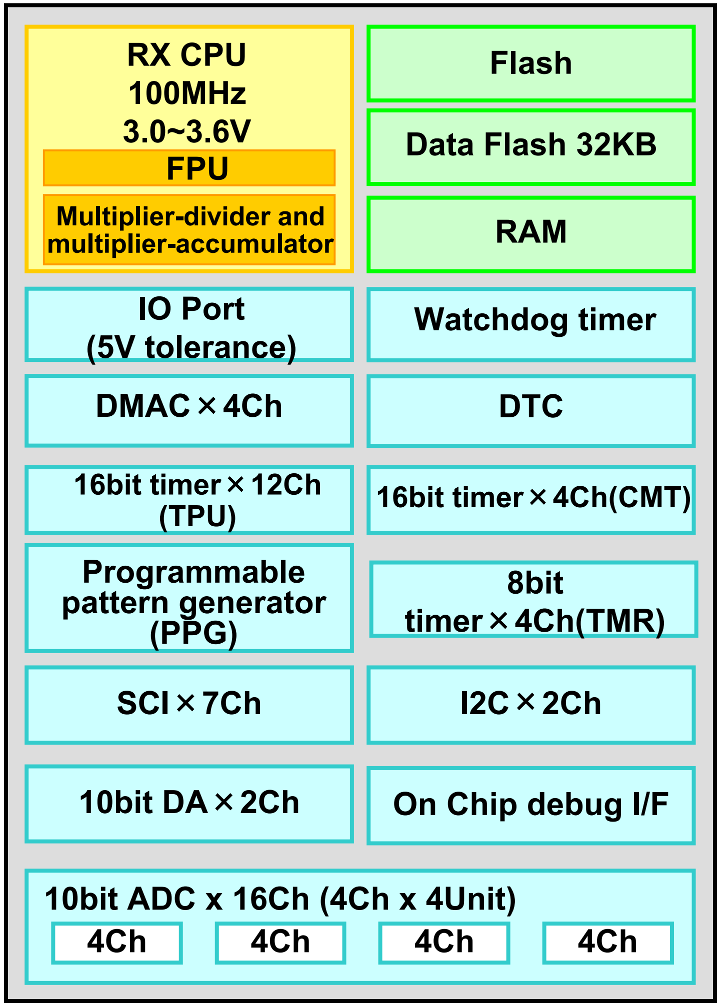
■ Product lineup

- ■ Nine products with wide selection of memory size and package
  - ■768kB Flash/128kB RAM to 2MB Flash/128kB RAM
  - ■144pin – 176pin package options

RX610 Group Specifications

- **High-performance CPU**
  - High-speed operation: Single-state basic instruction execution: 10ns
  - 100MHz@3.0 to 3.6V
  - 32bit multiplier/divider, multiplier-accumulator
  - single-precision FPU
- **On-chip memory**
  - Flash: 2 MB / RAM 128 KB
  - Flash: 1.5 MB / RAM 128 KB
  - Flash: 1 MB / RAM 128 KB
  - Flash: 768 KB / RAM 128 KB
- **Peripheral functions**
  - External bus expansion: 16-bit separate bus (ROM/RAM I/F, byte control SRAM I/F)
  - Transfer module: DMAC and DTC
  - Timers: High-performance general purpose timer: 16 bits x 12ch (TPU)
  - Timer optimized for OS and similar applications: 16 bits x 4ch (CMT)
  - General-purpose timer: 8 bits x 4ch (TMR)
  - High-speed 10-bit A/D converter (conversion time: 1μs)
  - 10-bit D/A converter x 2ch
  - Communication functions: Clock synchronous/asynchronous SCI x 7ch
  - I2C x 2ch (Fast-mode Plus)
- **Development environment**
  - On-chip debug emulator
  - Full emulator
- **Package**
  - LQFP144, BGA176-pin

RX610 Group Block Diagram



RX610 Product Lineup

Flash / RAM	144 pins LQFP	176 pins LFBGA
2MB / 128KB	R5F56108V ★	R5F56108W ★★
1.5MB / 128KB	R5F56107V ★	R5F56107W ★★
1MB / 128KB	R5F56106V ★	R5F56106W ★★
768KB / 128KB	R5F56104V ★	R5F56104W ★★

☆ : In planning
★★ : Under development
★ : New product

RX621 & RX62N Group

RX621 & RX62N Group Features

RX621
RX62N

Up to **512kB** Flash, **100MHz**, **12bit ADC, Ethernet, USB, CAN**

■ RX600 CPU

- ■ **High-speed (100MHz), high performance (1.65MIPS/MHz) and low current consumption (50mA@100MHz)**
- ■ **Single-precision floating point unit FPU, barrel shifter, MAC, RMPA**

■ Functions

- ■ **USB (Host/Function/OTG)**
- ■ **CAN**
- ■ **Ethernet MAC 10/100Mbit (RX62N)**
- ■ **12bit ADC (1 μs conversion time)**
- ■ **10-bit ADC (1 μs conversion time) x 2unit**
- ■ **10bit DAC 2 channel**
- ■ **Extreme number of communication functions (SCI: 6 ch, I2C(1Mbps), RSPI (18MHz))**
- ■ **Large number of timer functions (16-bit timer x 16 ch, 8-bit timer x 4 ch, Motor control Timer MTU2)**
- ■ **Zero wait access to Flash memory**

■ Product lineup

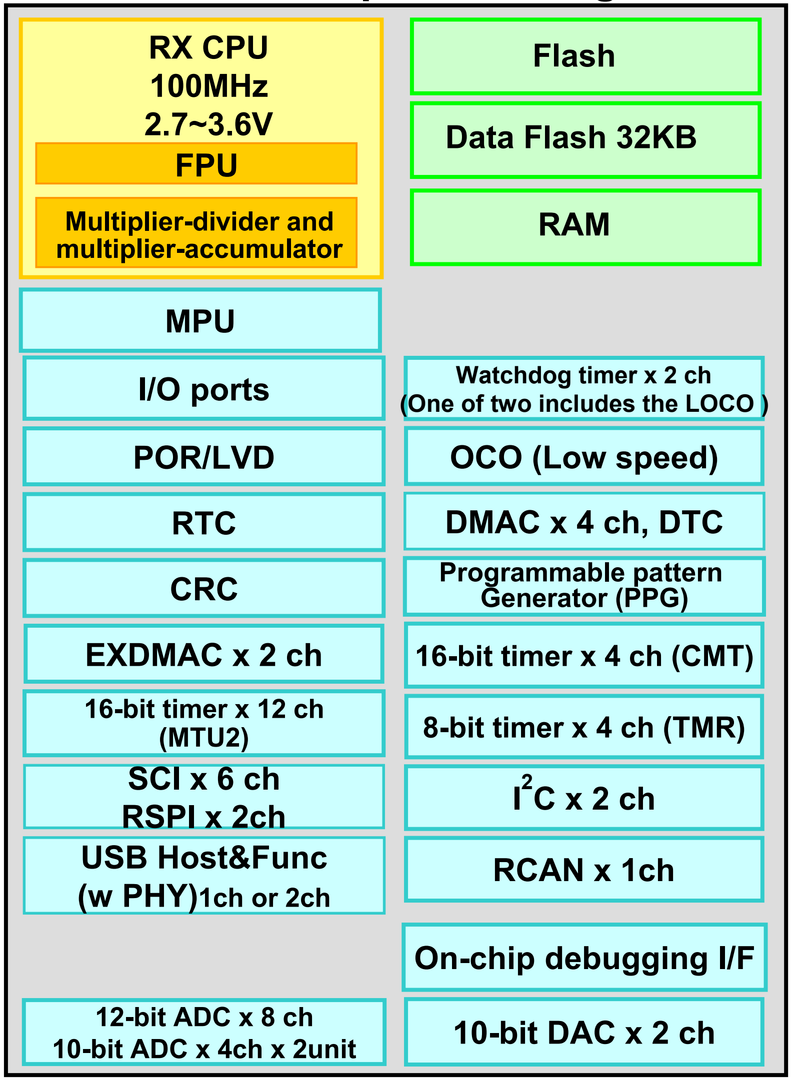
- ■ **Large products line-up with wide selection of memory size and package**
  - ■ **512kB Flash/96kB RAM to 256kB Flash/64kB RAM**
  - ■ **85pin – 176pin package options**

RX621 Group Specifications

Under Development

- **High-performance CPU**
  - High-speed operation: Single-state basic instruction execution: 10ns
  - 100MHz@2.7 to 3.6V
  - 32bit multiplier/divider, multiplier-accumulator
  - single-precision FPU
  - **On-chip memory with MPU**
  - Flash: 512 kB / RAM: 96 KB
  - Flash: 384 kB / RAM: 64 KB
  - Flash: 256 kB / RAM: 64 KB
- **Peripheral functions**
  - USB 2.0 (Host/Function/OTG)
  - CAN
  - Transfer module: DMAC and DTC
  - Timers: High-performance Motor timer: 16 bits x 12ch (MTU2)
  - Timer optimized for OS and similar applications: 16 bits x 4ch (CMT)
  - General-purpose timer: 8 bits x 4ch (TMR)
  - High-speed 10-bit A/D converter (conversion time: 1μs) 2units
  - High-speed 12-bit A/D converter (conversion time: 1μs)
  - 10-bit D/A converter x 2ch
  - Communication functions: Clock synch/asynch SCI x 6ch
  - I2C x 2ch (Fast-mode Plus)
  - RTC
  - EXDMAC for TFT-LCD Direct drive
  - Improved functions for the safety of the system:
    - POR, LVD, I-WDT, MPU
- **Development environment**
  - On-chip debug emulator
- **Package**
  - LGA85, LQFP100, LQFP144, LGA145, BGA176-pin

RX621 Group Block Diagram



RX62N Group Specifications

Under Development

■ **High-performance CPU**
- High-speed operation: Single-state basic instruction execution: 10ns
- 100MHz@2.7 to 3.6V
- 32bit multiplier/divider, multiplier-accumulator
- single-precision FPU

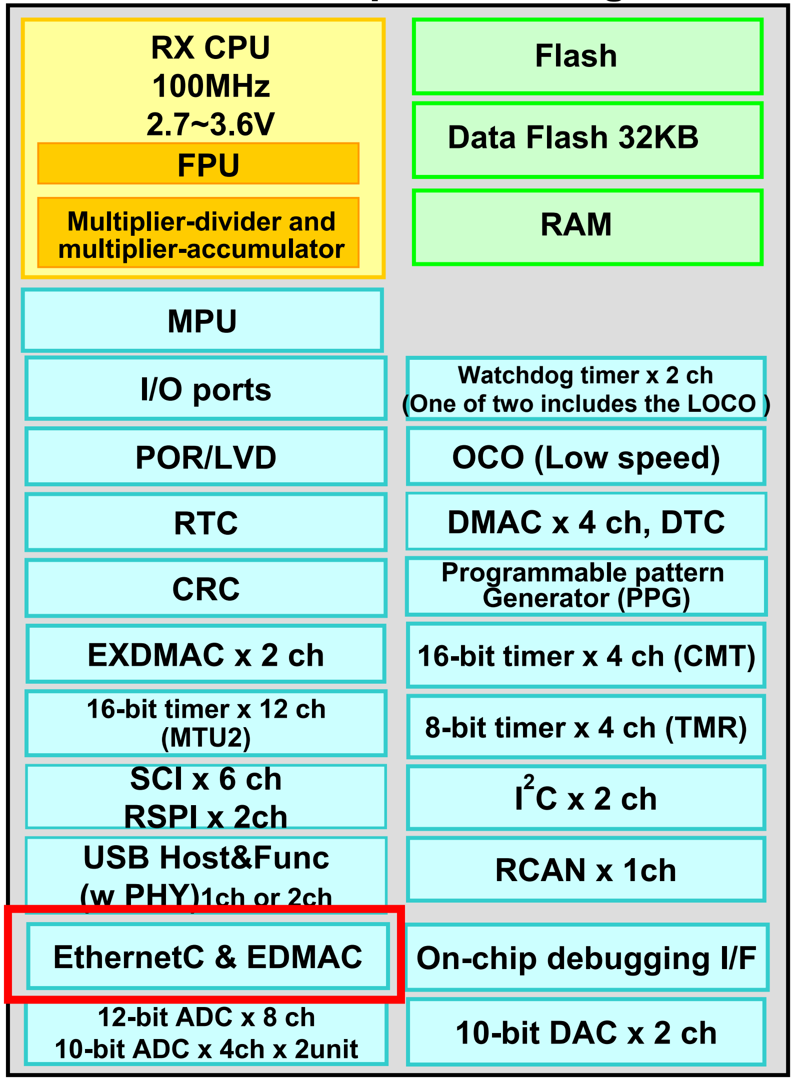
■ **On-chip memory with MPU**
- Flash: 512 kB / RAM: 96 KB
- Flash: 384 kB / RAM: 64 KB

■ **Peripheral functions**
- USB 2.0 (Host/Function/OTG)
- CAN (optional)
- Ethernet MAC with EDMAC
- Transfer module: DMAC and DTC
- Timers: High-performance Motor timer: 16 bits x 12ch (MTU2)
- Timer optimized for OS and similar applications: 16 bits x 4ch (CMT)
- General-purpose timer: 8 bits x 4ch (TMR)
- High-speed 10-bit A/D converter (conversion time: 1μs) 2units
- High-speed 12-bit A/D converter (conversion time: 1μs)
- 10-bit D/A converter x 2ch
- Communication functions: Clock synch/asynch SCI x 6ch
- I2C x 2ch (Fast-mode Plus)
- RTC
- EXDMAC for TFT-LCD Direct drive
- Improved functions for the safety of the system:
  - POR, LVD, I-WDT, MPU

■ **Development environment**
- On-chip debug emulator

■ **Package**
- LQFP100, LQFP144, LGA145, BGA176-pin

RX62N Group Block Diagram



RX621 & RX62N Group Benefits

RX62N the perfect fit choice

	Needs to MCUs	Advantages/Benefit
High integration	Network - Ether, USB, CAN -	High integration, ensured reliability
	Security - Flash Protection, CRC -	Ensured reliability from end users
High performance	High speed communication - Gateway -	High speed access to the center for reducing cost
	High speed Human I/F - Higher speed ADC -	No waiting time for customers
Low cost	Flexibly corresponds - Various memory line up -	Reduce development costs
	LCD display - LCD Direct Drive -	No need for LCD controller chip

External parts are eliminated by RX62N

High integration

- Extensive network functions

  RX62N : Ether, USB (Host/Device), CAN

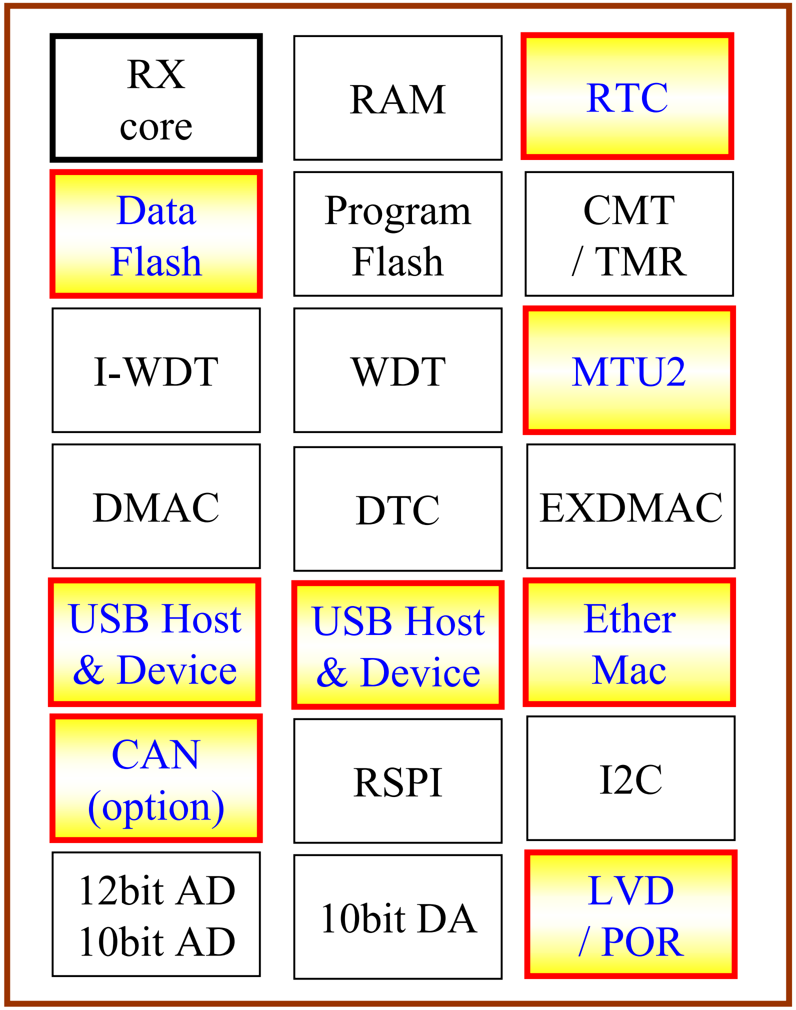
  RX621 : USB (H/D), CAN (Option)

  : IIC x2ch, RSPI x2ch, SCI x6ch

- Reduce external devices

  - Data Flash : No need EEPROM
  - POR/LVD : No need Reset circuit
  - RTC : Full calendar supported
  - MTU2 : Reduce external circuit for motor application

RX62N group

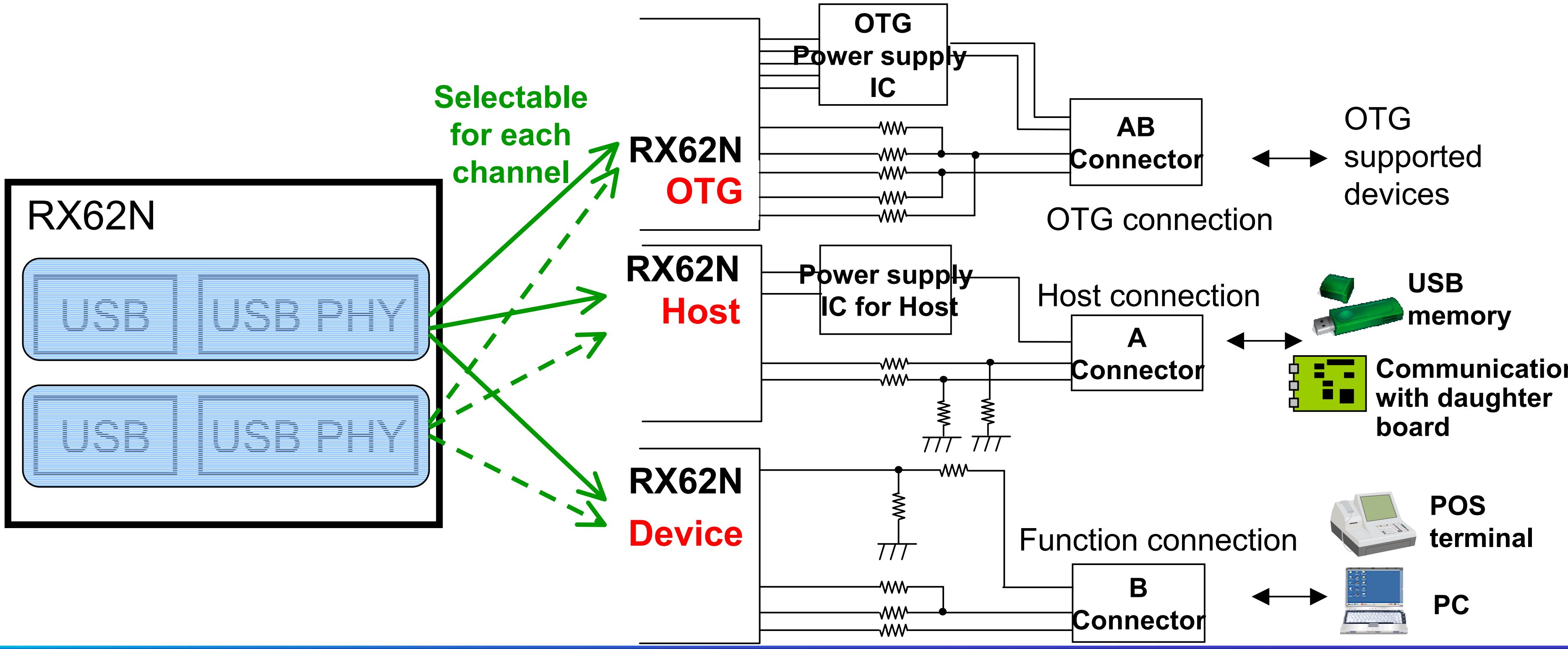


Connectivity Features - USB Function -

RX62N
RX621

High Integration

- Proven USB module (R8A66597) is embedded.
- Independent two-unit USB is embedded for 176pin
- Host/Device/OTG can be selected for each unit.
- Interrupt/bulk/control/isochronous transfer are supported.
- External circuit with high reliability is provided (USB logo is easily taken).



Connectivity Features - Ethernet Function -

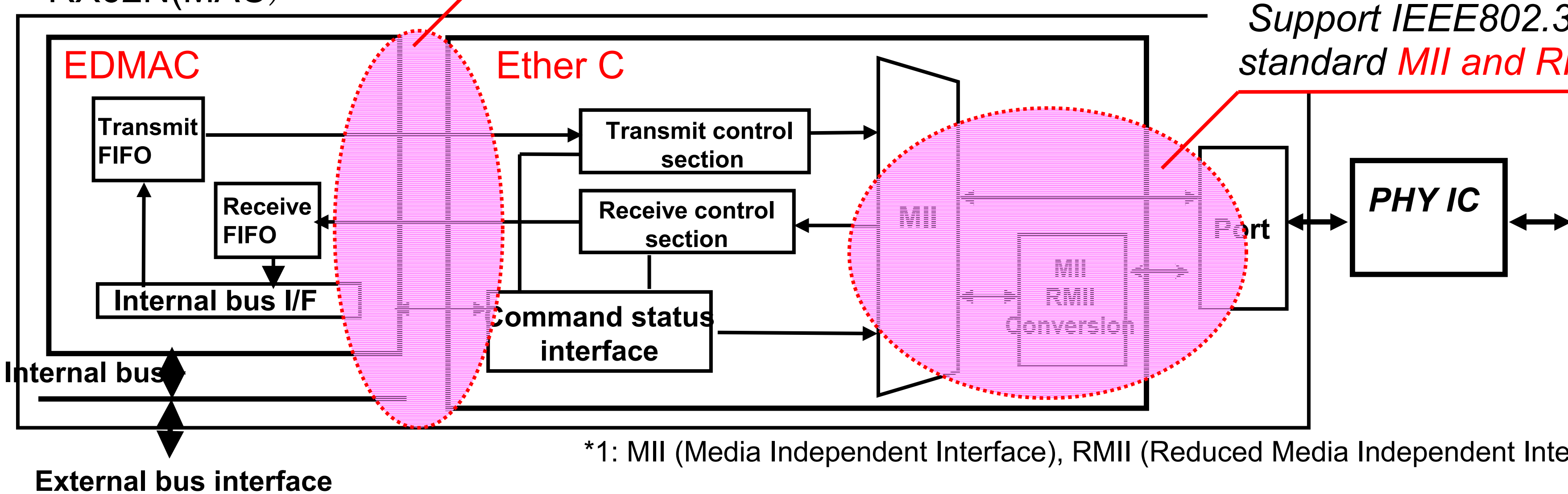
RX62N

High Integration

- Common Ether used for SuperH and H8S is used.
- The know-how of external circuit (including PHY) can be utilized.
- Driver software is provided considering continuity from SuperH.
- 10/100 Base Ether Transfer (IEEE802.3)

Embedded EDMAC for EtherC
Reduces CPU load and efficient transmitting and receiving data

Support IEEE802.3u-standard MII and RMII



*1: MII (Media Independent Interface), RMII (Reduced Media Independent Interface)

How to get the high system throughput

High performance

- High speed communication

  Multi internal bus for parallel operation

  - DMA and DTC transfer

  - CPU bus

- High speed Human interface

  High speed 10bit ADC inside

  - Easy to realize the highest sampling rate by 2unit

- Connect to various sensors

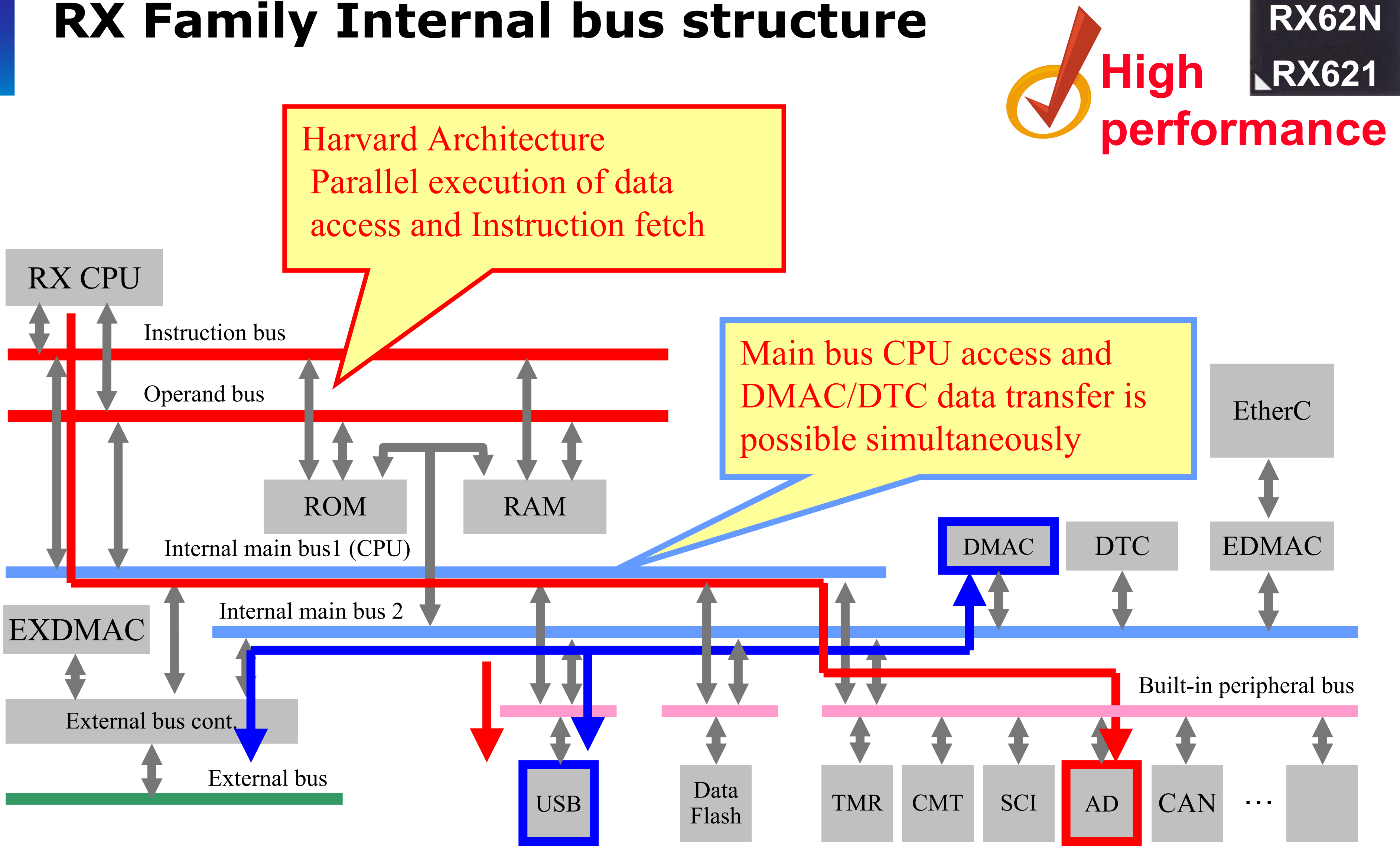
  High resolution 12bit ADC inside

  - Easy to use the positioning sensor, etc

RX62N group

RX core	RAM	RTC
Data Flash	Program Flash	CMT / TMR
I-WDT	WDT	MTU2
DMAC	DTC	EXDMAC
USB Host & Device	USB Host & Device	Ether Mac
CAN (option)	RSPI	I2C
12bit AD 10bit AD	10bit DA	LVD / POR

RX Family Internal bus structure



High speed and High resolution ADC

RX62N
RX621

- High speed 10bit A/D convertor x 2 units

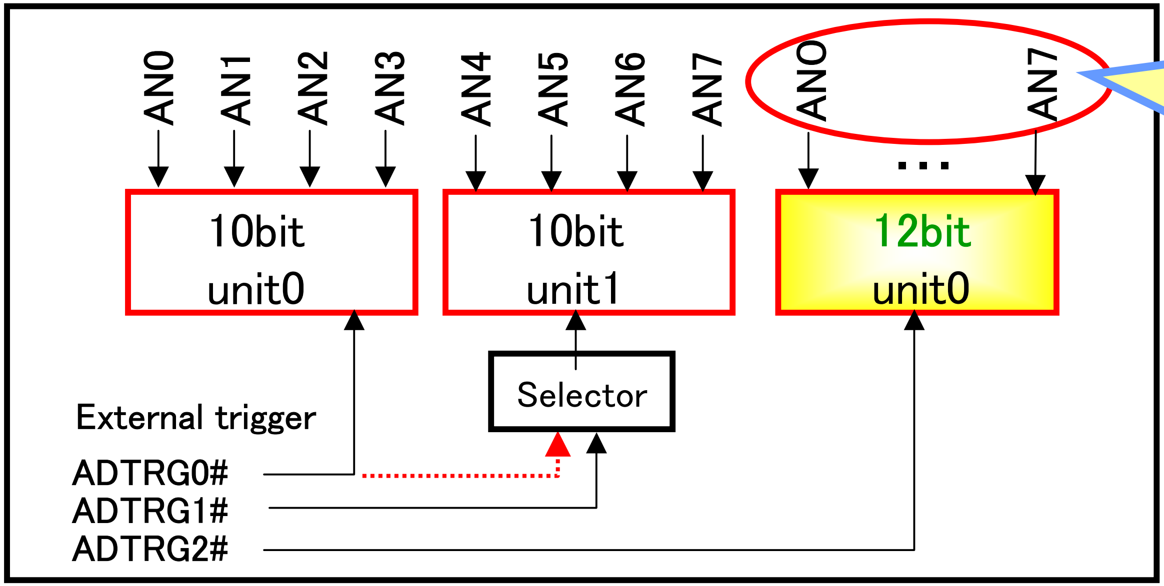
or

- High resolution12bit A/D convertor x 1 unit

< Future >

- 1us sampling rate by 10bit and 12bit ADC
- each other ADC is operated independently
- 2 unit ADC can operate by same external trigger(ADTRG0#)

High performance



Shared pin assignment between 10bitADC and 12bit ADC

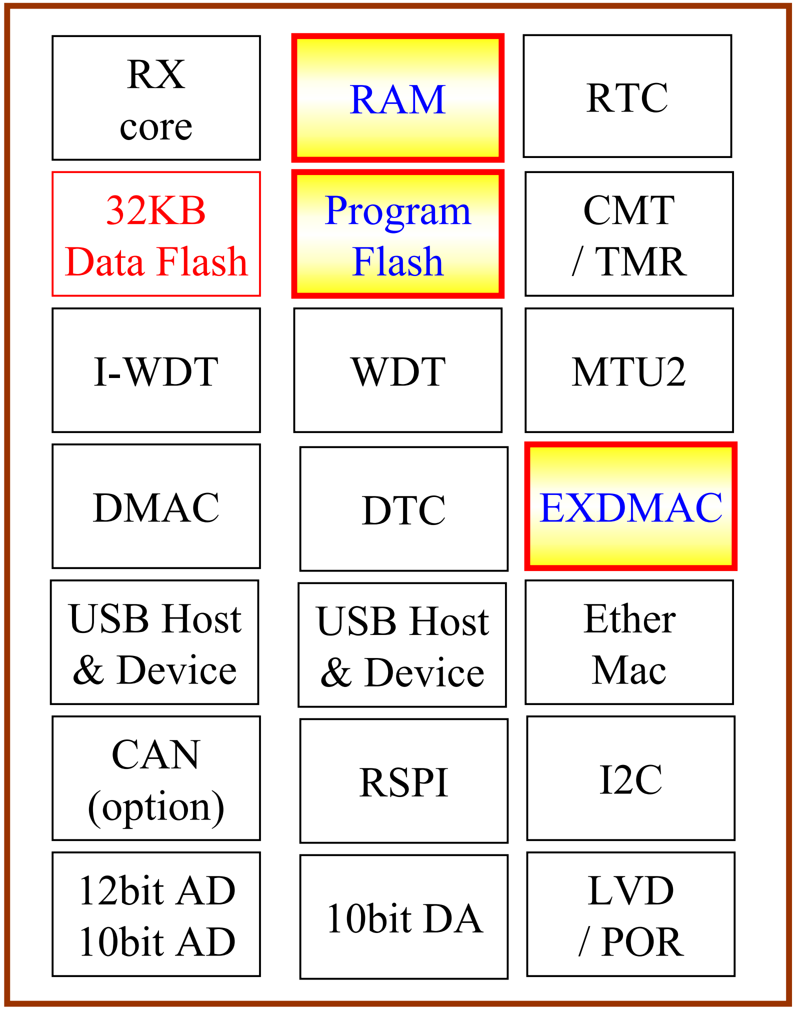
To reduce the system cost

Low cost

- For common PCB design
  - A lot of memory variation
    with pin compatible
    256KB Flash, 64KB RAM
    384KB Flash, 64KB RAM
    512KB Flash, 96KB RAM
  - A lot of PKG variation
    to choose the suitable one
    100, 144pin LQFP
    85, 145pin LGA
    176pin BGA

- LCD display
  LCD Direct Drive solution by EXDMAC

RX62N group



RX621 & RX62N Product Lineup

☆ : In planning
★★ : Under development
★ : New product

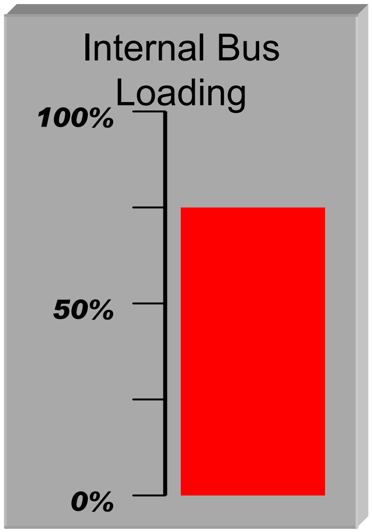
Flash / RAM	85 pins LGA	100 pins LQFP	144 pins LQFP	145 pins LGA	176 pins LFBGA	Feature
512kB/96KB		R5F562N8BxFP ★★	R5F562N8BxFB ★★	R5F562N8BxLD ★★	R5F562N8BxBG ★★	Ethernet, USB, CAN
		R5F562N8AxFP ★★	R5F562N8AxFB ★★	R5F562N8AxLD ★★	R5F562N8AxBG ★★	Ethernet, USB
	R5F56218BxLD ★★	R5F56218BxFP ★★	R5F56218BxFB ★★	R5F56218BxLD ★★	R5F56218BxBG ★★	USB, CAN
384kB/64KB		R5F562N7AxFP ★★	R5F562N7AxFB ★★	R5F562N7AxLD ★★	R5F562N7AxBG ★★	Ethernet, USB, CAN
		R5F562N7BxFP ★★	R5F562N7BxFB ★★	R5F562N7BxLD ★★	R5F562N7BxBG ★★	Ethernet, USB
	R5F56217BxLD ★★	R5F56217BxFP ★★	R5F56217BxFB ★★	R5F56217BxLD ★★	R5F56217BxBG ★★	USB, CAN
256KB/64KB	R5F56216BxLD ★★	R5F56216BxFP ★★	R5F56216BxFB ★★	R5F56216BxLD ★★	R5F56216BxBG ★★	USB, CAN

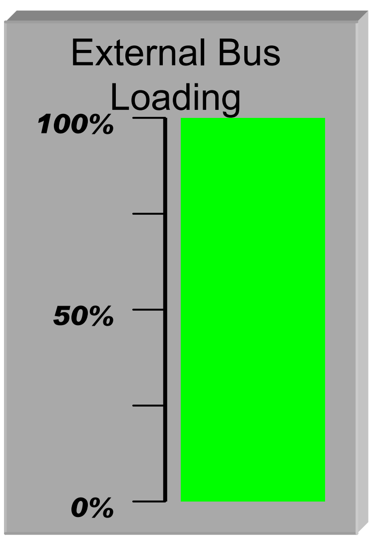
LCD Direct Drive solution by EXDMAC

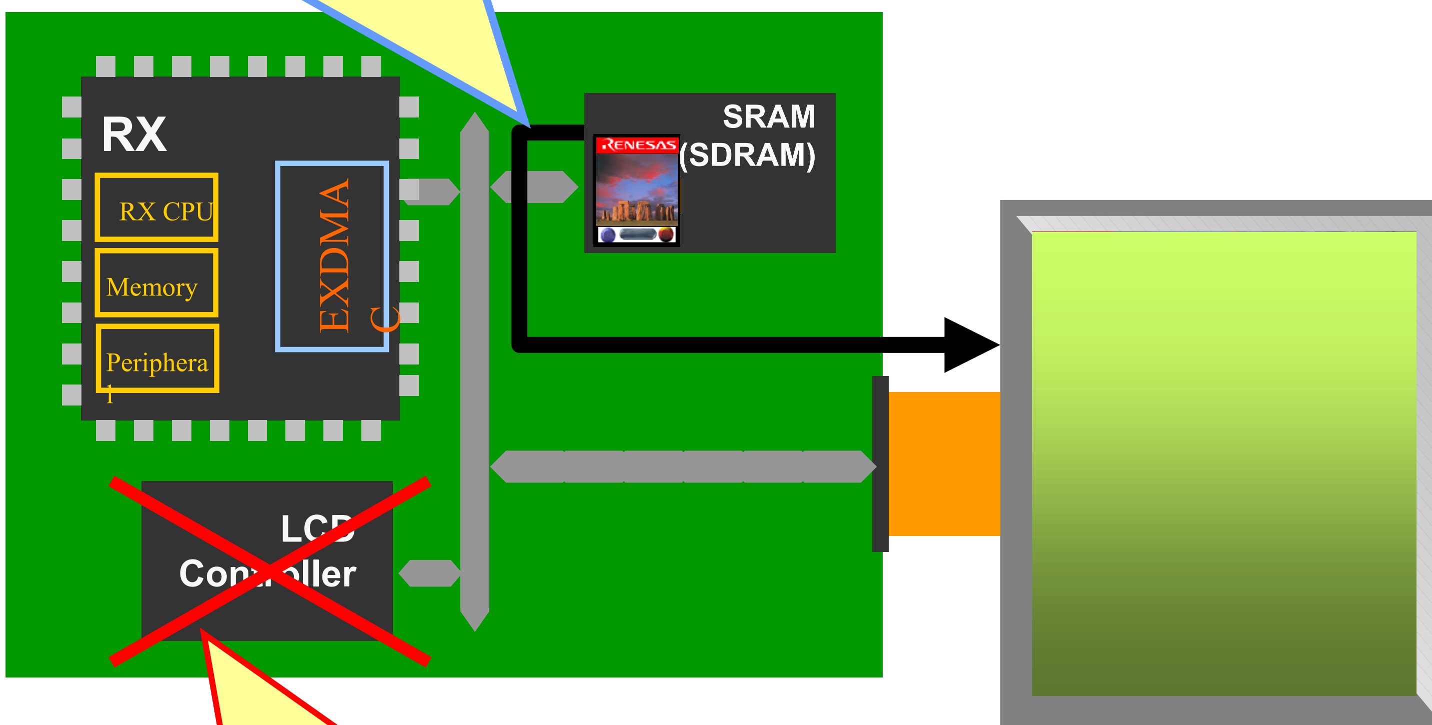
RX62N
RX621

Low cost

< EXDMAC >
Since EXDMAC supports LCD display, CPU load great is reduced.







< Reduce the cost >
No need external LCD Controller

Full Screen animation at ***25*** frames per second

RX62T Group

RX62T Group Features

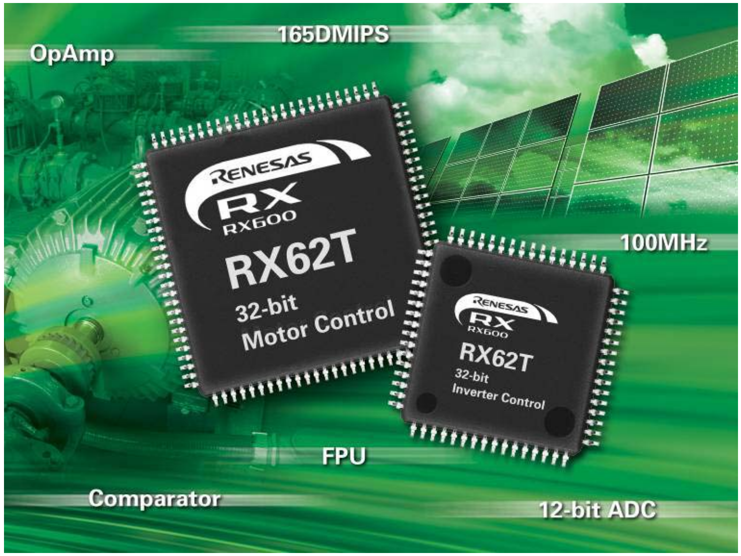
RX62T Up to **256kB** Flash, **100MHz**, **two motor** control timers, **12bit ADC, OpAmp ,CAN** option

RX600 CPU

- High-speed (100MHz), high performance (1.65MIPS/MHz) and low current consumption (50mA@100MHz)
- Single-precision floating point unit FPU, barrel shifter, MAC, RMPA

Functions

- Enhanced PWM resolution with MTU3
- Enhanced PWM functionality with GPT
- 12bit ADC(1us): 4ch x 2 unit, 10bit ADC(1us):12ch x 1 unit
- Three S/H circuits for each unit → 3 shunt control
- Double data registers for each unit → 1 shunt control
- Programmable gain amplifier
- Window comparator for Voltage monitoring
- CAN option
- Released two type products (3.3 and 5.0V) for each line up
- Pin to pin compatible between 3.3V and 5.0V products
- Zero wait access to Flash memory



Product lineup

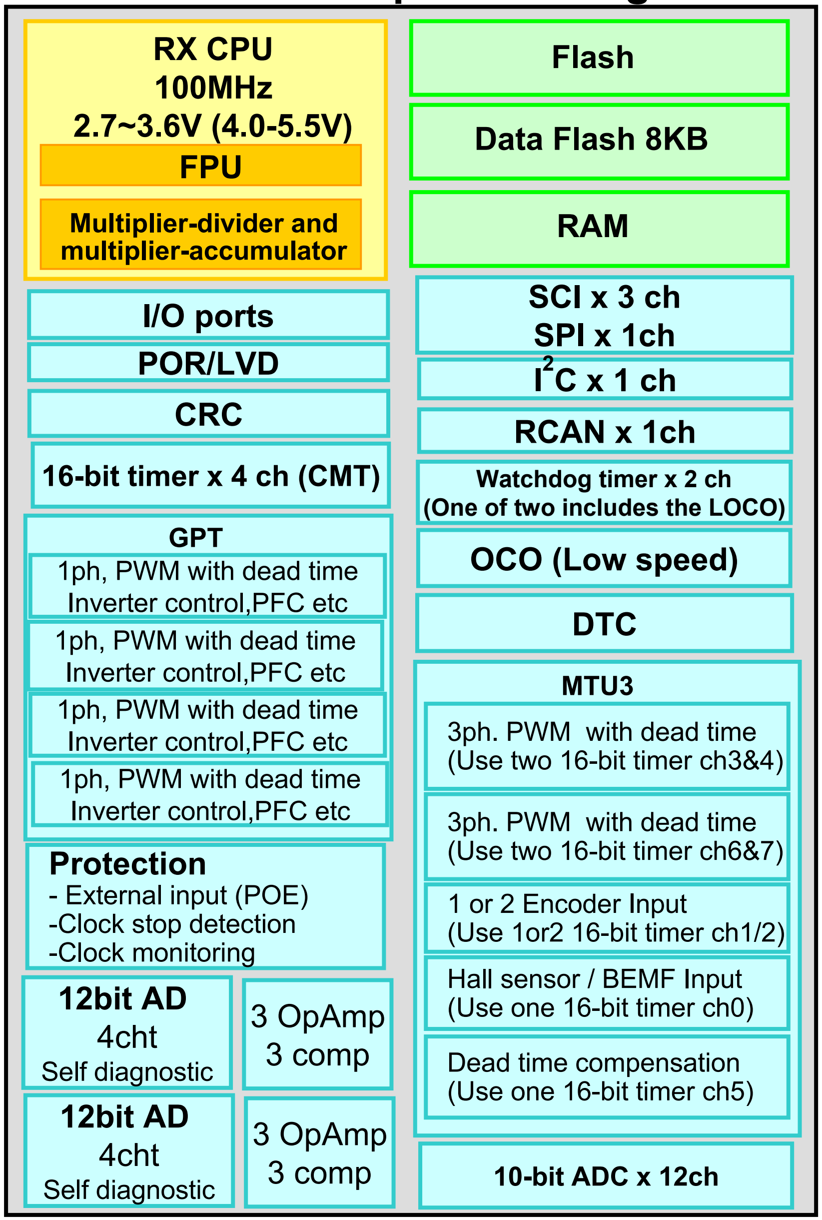
- Large products line-up with wide selection of memory size and package
  - 256kB Flash/16kB RAM to 64kB Flash/8kB RAM
  - 64pin – 112pin package options

Under Development

RX62T Group Specifications

- **High-performance CPU**
  - High-speed operation: Single-state basic instruction execution: 10ns
  - 100MHz@2.7 to 3.6V and 4.0 to 5.5V
  - 32bit multiplier/divider, multiplier-accumulator
  - single-precision FPU
- **On-chip memory**
  - Flash: 256 kB / RAM: 16 KB
  - Flash: 128 kB / RAM: 8 KB
  - Flash: 64 kB / RAM: 8 KB
- **Peripheral functions**
  - Timer MTU3: High-performance Motor timer
    - To control two 3ph. motors with dead time insertion
  - Timer GPT: PFC and 1ph Motor control timer
  - Timer optimized for OS and similar applications: 16 bits x 4ch (CMT)
  - High-speed 12-bit A/D converter (conversion time: 1μs) with OpAmp and comparator
  - High-speed 10-bit A/D converter (conversion time: 1μs) with self diagnostic
  - CAN (option)
  - Transfer module: DTC
  - General-purpose timer: 8 bits x 4ch (TMR)
  - Communication functions: Clock synch/asynch SCI x 3ch
  - I2C x 1ch (Fast-mode Plus)
  - Improved functions for the safety of the system:
    - POE, POR, LVD, I-WDT
- **Development environment**
  - On-chip debug emulator
- **Package**
  - LQFP64, LQFP80, LQFP100, LQFP112

RX62T Group Block Diagram



RENESAS

RX62T Product Lineup

☆ : In planning
★★ : Under development
★ : New product

Flash / RAM	Feature	Voltage	64 pins LQFP	80 pins LQFP	100 pins LQFP	112 pins LQFP
256kB/16KB	1ch CAN	5V	R5F562T7A[1] ★★	R5F562T7A ★★	R5F562T7A ★★	R5F562T7A ★★
		3.3V	R5F562T7B ★★	R5F562T7B ★★	R5F562T7B ★★	R5F562T7B ★★
	non CAN	5V	R5F562T7D[1] ★★	R5F562T7D ★★	R5F562T7D ★★	R5F562T7D ★★
		3.3V	R5F562T7E ★★	R5F562T7E ★★	R5F562T7E ★★	R5F562T7E ★★
128kB/8KB	1ch CAN	5V	R5F562T7A[1] ★★	R5F562T7A ★★	R5F562T7A ★★	R5F562T7A ★★
		3.3V	R5F562T7B ★★	R5F562T7B ★★	R5F562T7B ★★	R5F562T7B ★★
	non CAN	5V	R5F562T7D[1] ★★	R5F562T7D ★★	R5F562T7D ★★	R5F562T7D ★★
		3.3V	R5F562T7E ★★	R5F562T7E ★★	R5F562T7E ★★	R5F562T7E ★★
64KB/8KB	1ch CAN	5V	R5F562T6A[1] ★★	R5F562T6A ★★		
		3.3V	R5F562T6B ★★	R5F562T6B ★★		
	non CAN	5V	R5F562T6D[1] ★★	R5F562T6D ★★		
		3.3V	R5F562T6E ★★	R5F562T6E ★★		

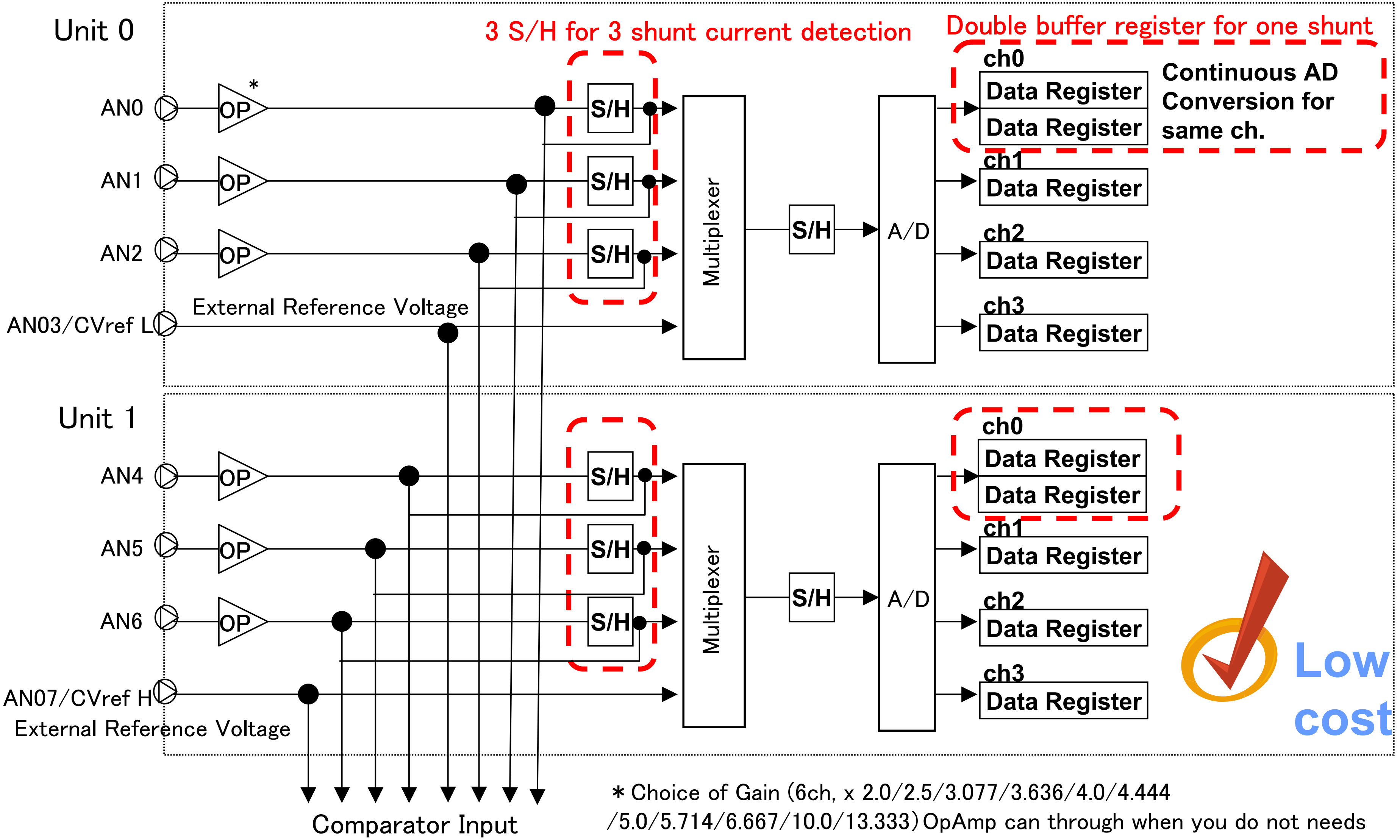
[1]: 80MHz

RX62T Group Benefits

12bit A/D Configuration with OpAmp

RX62T

■Each unit have same functionality. Supporting one shunt or Three shunt current detection

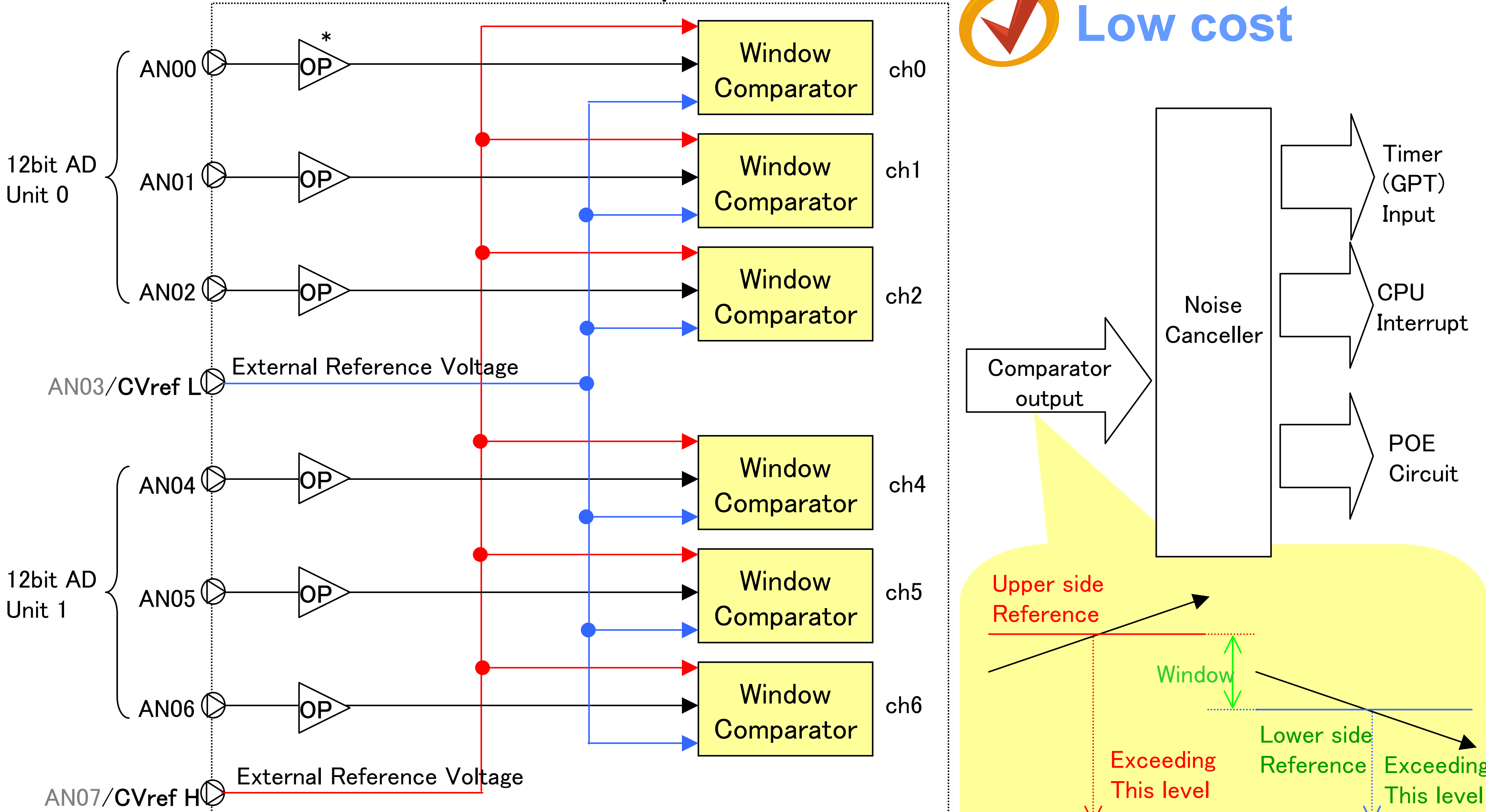


＊Choice of Gain (6ch, x 2.0/2.5/3.077/3.636/4.0/4.444/5.0/5.714/6.667/10.0/13.333) OpAmp can through when you do not needs

Comparator configration

RX62T

■Each 12bitAD has window three comparator



＊Choice of Gain (6ch, x 2.0/2.5/3.077/3.636/4.0/4.444/5.0/5.714/6.667/10.0/13.333)
OpAmp can through when you do not needs

Multi Function Timer for Inverter Control (MTU3)

RX62T

High performance

Features

- Eight 16bit counter
- Max. 24 pulse input/output, and 3 input
- It can feed up to 100MHz
- Operation Mode
  - Output compare match (Low,High,toggle)
  - Input capture
  - Synchronous operation: Multiple timer synchronies simultaneous clear by compare match or input capture
  - PWM Mode: 0 to 100% duty PWM output
  - Encoder counting

Motor Related function

(Use ch3&4 as a pare, ch6&7 as well)

Types of PWM waveform

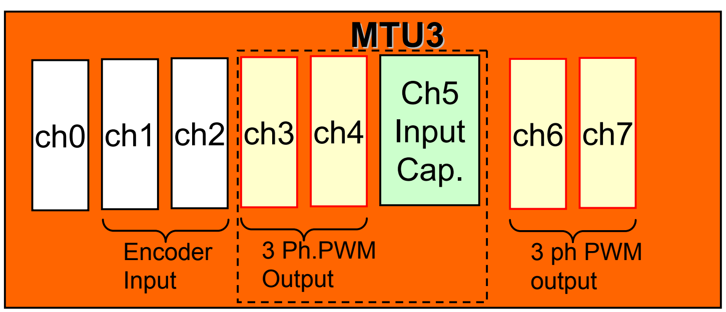
– Reset synchronous PWM mode: saw tooth PWM wave
– Complementary PWM mode: Triangle waveform
– Dead time are automatically insert

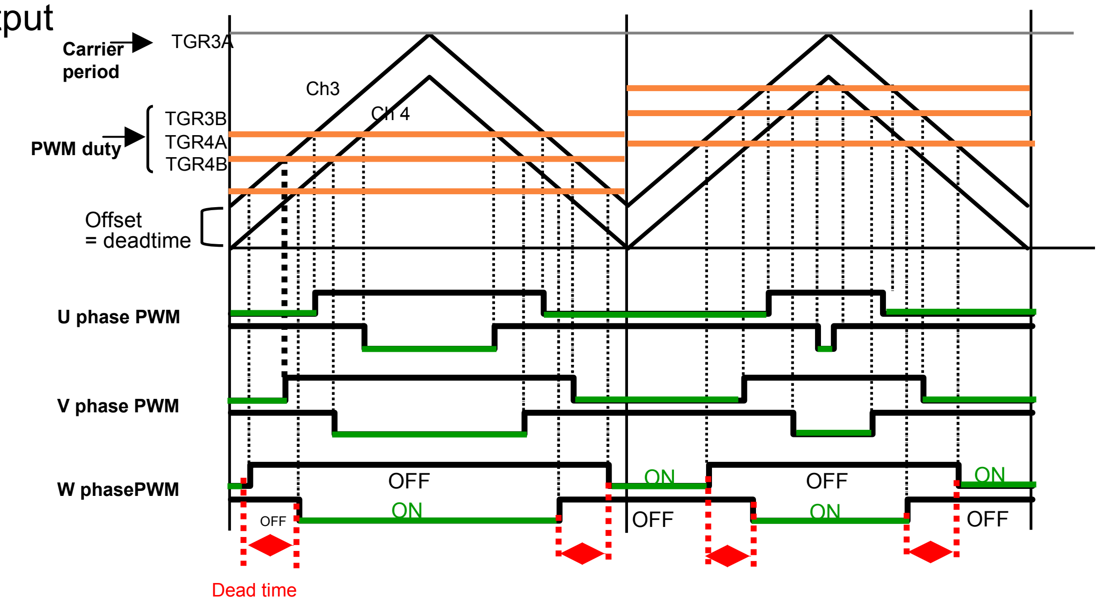
Interrupt skip function

– It is able to skip interrupt request up to seven times

AD conversion trigger

– There are two register you could set up a trigger timing of AD





RENESAS

General PWM Timer (GPT)

- Functions
  - Up, down or up/down counting selectable for each counter
  - Clock sources independently selectable for each channel
  - Generation of laterally asymmetric PWM waveforms.
  - Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow)
  - Synchronizable operation of several counters
  - Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting)
  - Generation of dead times in PWM operation
  - Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times
  - Starting, clearing, and stopping counters in response to
    - Internal trigger sources: output of the internal comparators, software, and compare match
    - External trigger sources: capture input and dedicated trigger input

- Features
  - Operates at up to 100 MHz
  - 4 x 16-bit Timer Unit Register blocks
  - 2x4 input/output pins
  - 2x4 compare match / input capture registers
  - 4x4 compare match registers
  - Up to 4 pre-scaled internal input clocks

IEC60730＊[1] Corresponding

RX62T

IEC60730 Item＊2	Corresponding feature of ＲＸ６２Ｔ
Interrupt handling and execution	Monitoring by Independent Watchdog Timer with Checker software.
Clock	Clock stop detection and clock delay monitor
External communication	CRC(Cyclic Redundancy Check)on chipped
Input/Output periphery	Always port value are readable Even it are selected as peripheral function
A/D converter	Provide three level(Avreff,1/2AV ref, AVrefss) for self test

＊１ International fail safe standard

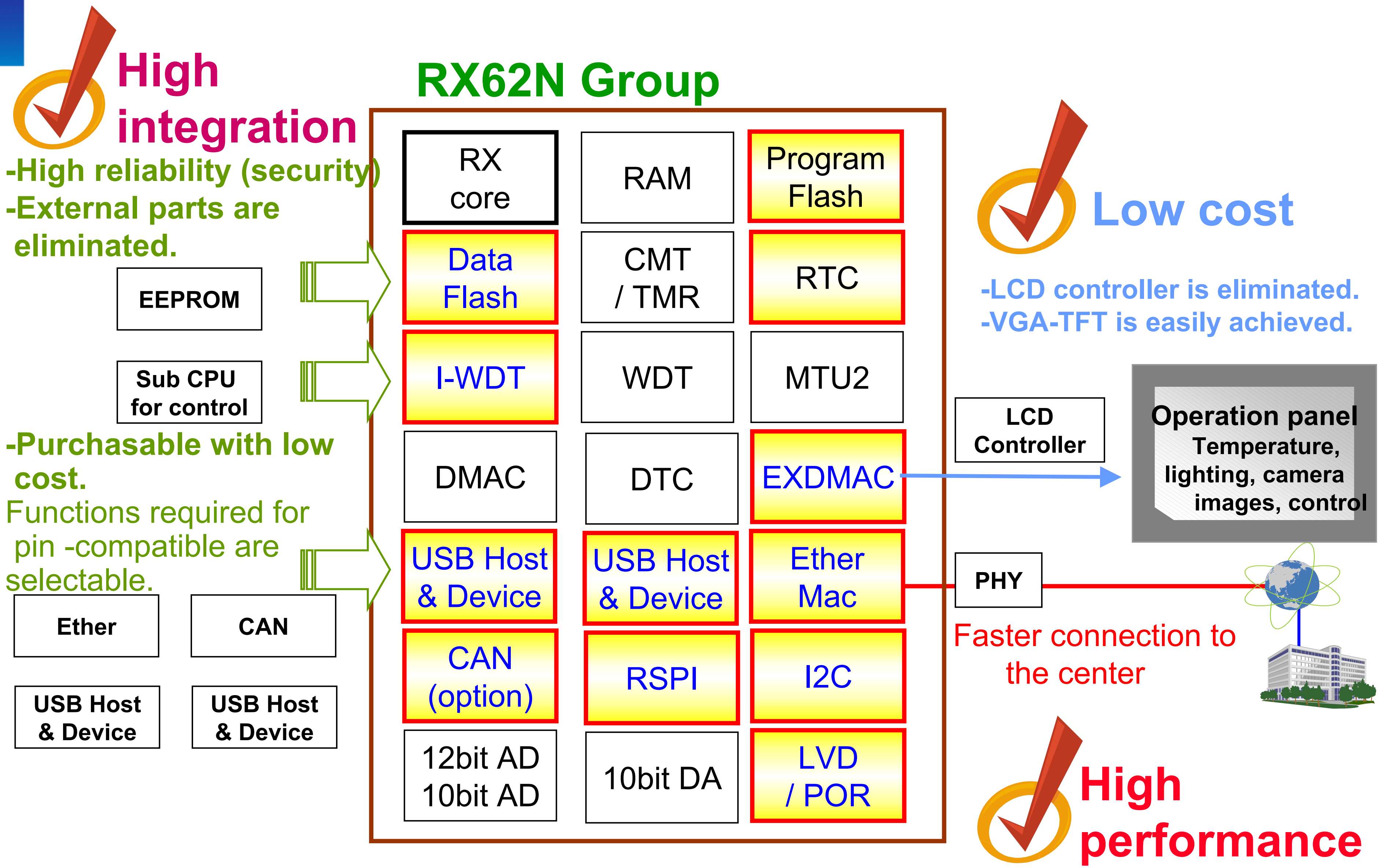
＊２ Not all of IEC60730

RX62T Motor Reference Platform

- We can provide following information for quick & easy developments together with our alliance partner BFG
  - Application notes
  - Sample program
  - BOM List
  - Circuit diagram
  - PC interface software for demo

RX Application Examples

Building Automation Application



Bar-code Scanner (POS system)

High integration

-High reliability (security)
Information protection,
prevent decoding

EEPROM

-Ensured reliability from end users
Embedded 2 unit USB
- I/F with POS terminal
- Information update with USB memory

USB Host & Device | USB Host & Device

-No waiting timer for customers
As twice bar-code scanning speed as previous products.

High performance

RX621 Group

RX core	RAM	Program Flash
Data Flash	CMT / TMR	RTC
I-WDT	WDT	MTU2
DMAC	DTC	EXDMAC
USB Host & Device	USB Host & Device	Ether Mac
CAN (option)	RSPI	I2C
12bit AD 10bit AD	10bit DA	LVD / POR

-High reliability (security)
Information protection,
prevent decoding
(Embedded MPU)

-Flexibility
Simplified connection to Bluetooth module etc

Bluetooth communication

Low cost

RESET IC

-Eternal parts are eliminated.

Digital Photo Frame or HMI

RX62N Group

High performance

JPEG middleware provided

High integration

-Easy image passing

Simplified connection to USB memory card or SD card

-Easy printing

USB and Ether are selectable

-Connection to various sensors

Selectable from 10-bit/12-bit depending upon purposes such as temperature sensor and accelerating sensor.

RX core	RAM	Program Flash
Data Flash	CMT / TMR	RTC
I-WDT	WDT	MTU2
DMAC	DTC	EXDMAC
USB Host & Device	USB Host & Device	Ether Mac
CAN (option)	RSPI	I2C
12bit AD 10bit AD	10bit DA	LVD / POR

Low cost

RTC IC

-Eternal parts are eliminated.

-LCD controller is eliminated.
-VGA-TFT is easily achieved.

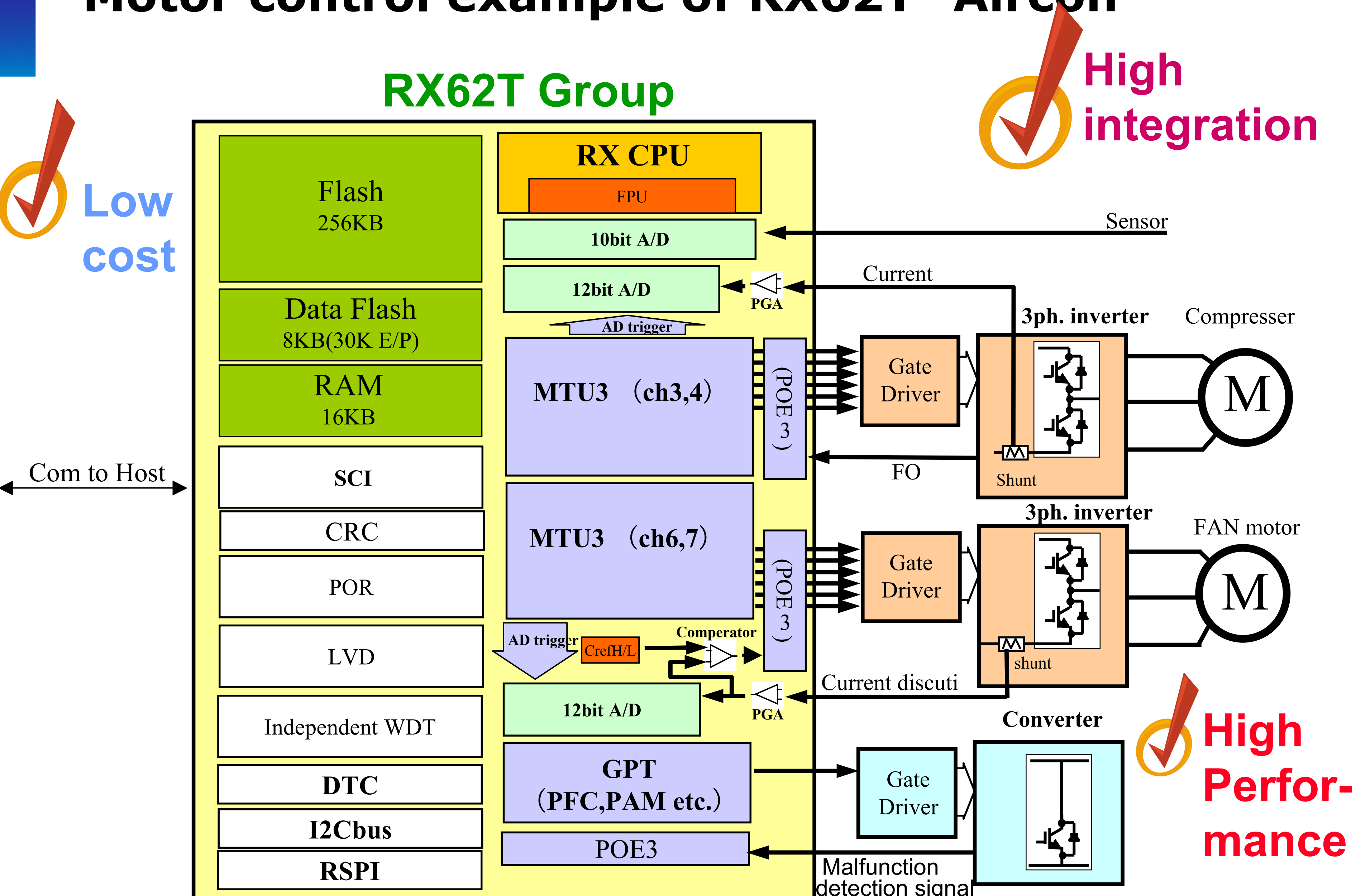
-Expansion

Simplified connection to Bluetooth module etc

RESET IC

-Eternal parts are eliminated.

Motor control example of RX62T -Aircon-

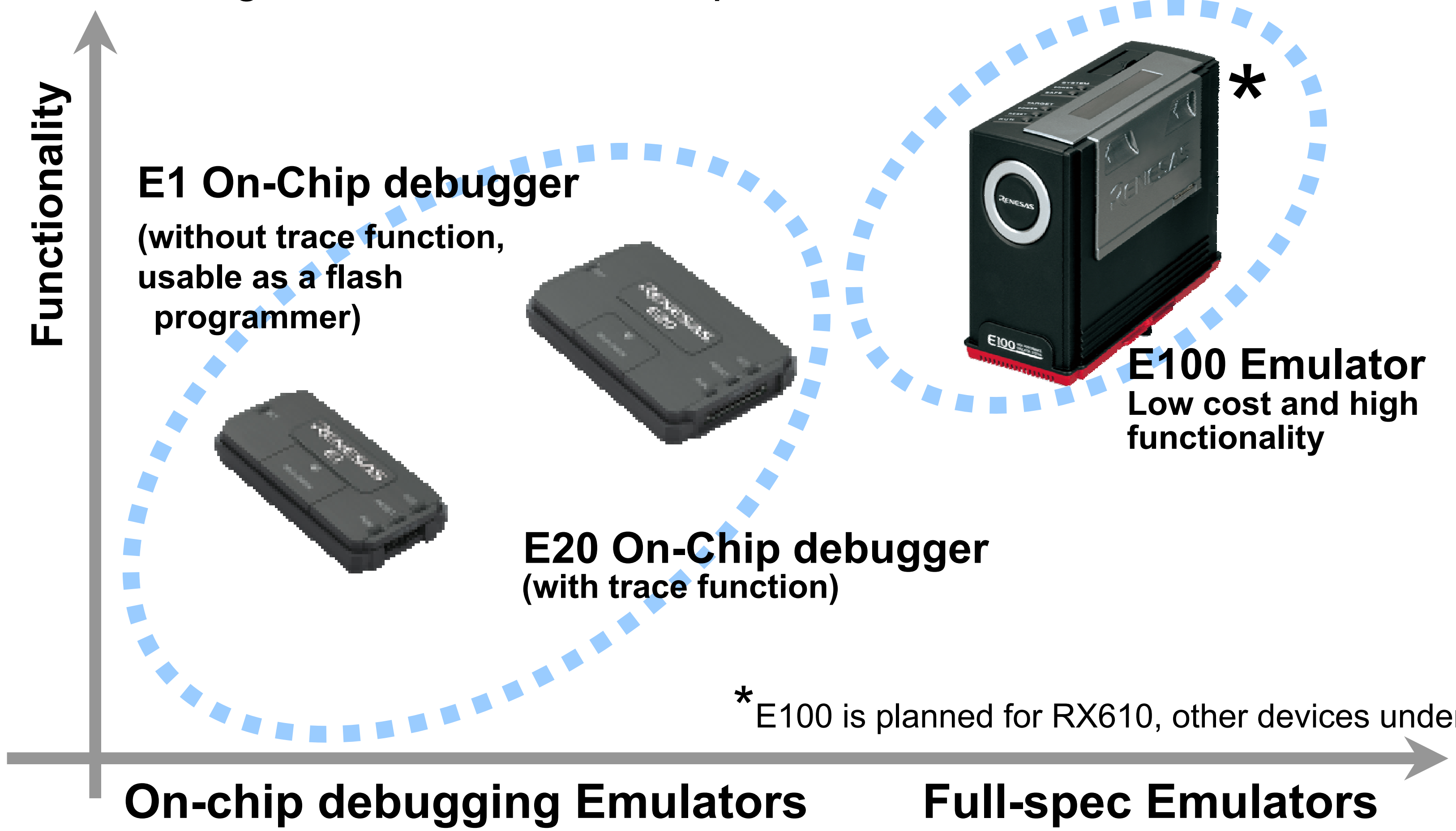


  REE-IBG-PM-BWE RENESAS

RX Development Tools

RX Platform Development Tools

- Emulator and debugger product lineup has been established to extensively support the RX Platform. The tools are best suited for the particular stage and scale of development can be selected.



*E100 is planned for RX610, other devices under review

Segger J-Link support for RX

- Segger ported their J-Link debugger to RX
- Segger do not develop debugger software and so plug into “third party” tools
  - IAR System Embedded Workbench
  - Renesas HEW
  - Eclipse

- Why are we doing this?
  - J-Link is virtually industry standard fro ARM debug
  - Having J-Link RX support available will make moving from ARM development to RX very easy.

- Any J-Link can be used, but a special 20-14 pin adapter is required

Compiler support for RX

Renesas RX Compiler

Integrated development environment using HEW4

IAR Systems RX C/C++ Compile

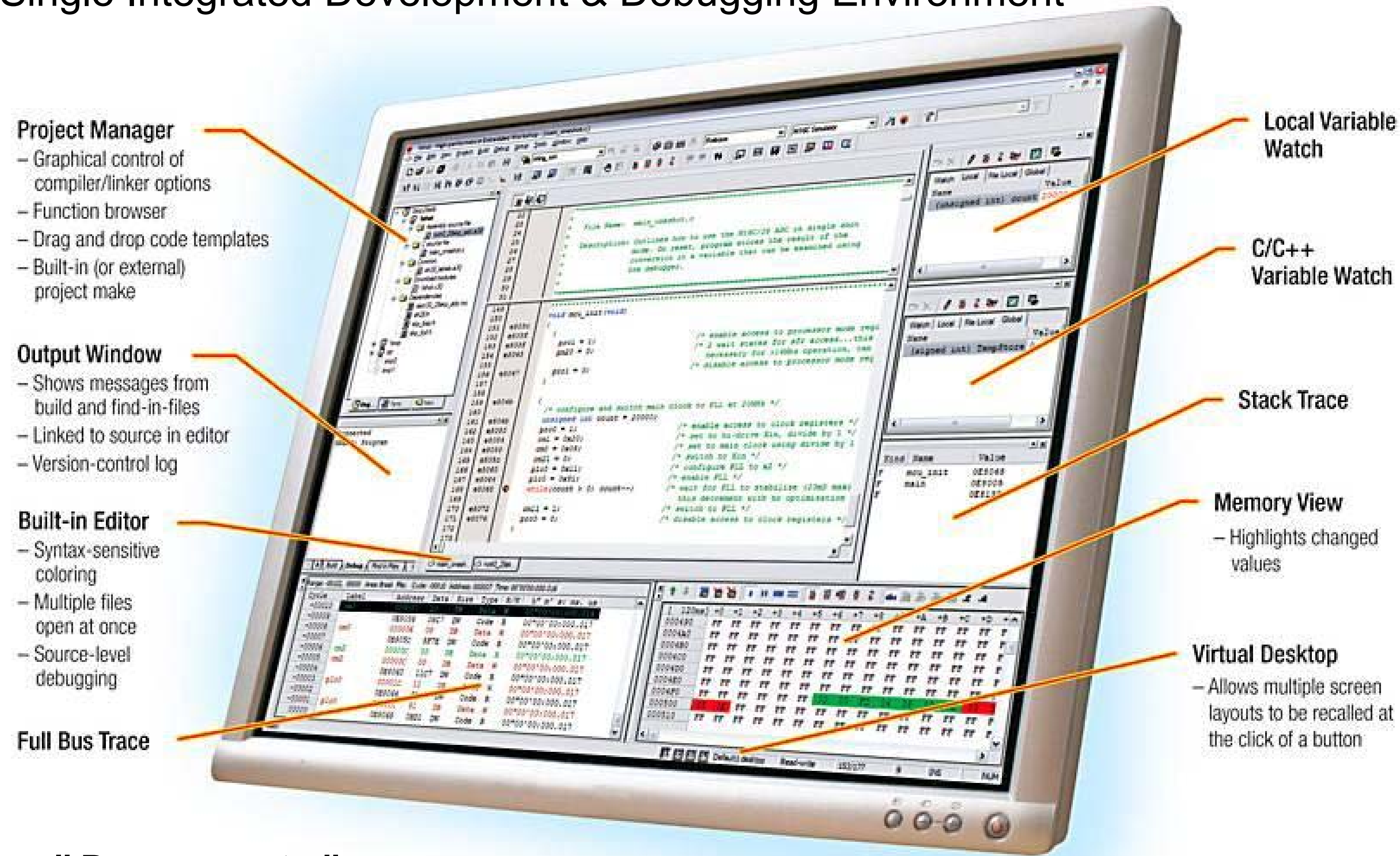
Integrated development environment ar
optimizing C/C++ compiler for RX

KPIT GNU compiler

FOC compiler for RX integrated to the HEW4 development environment

HEW4

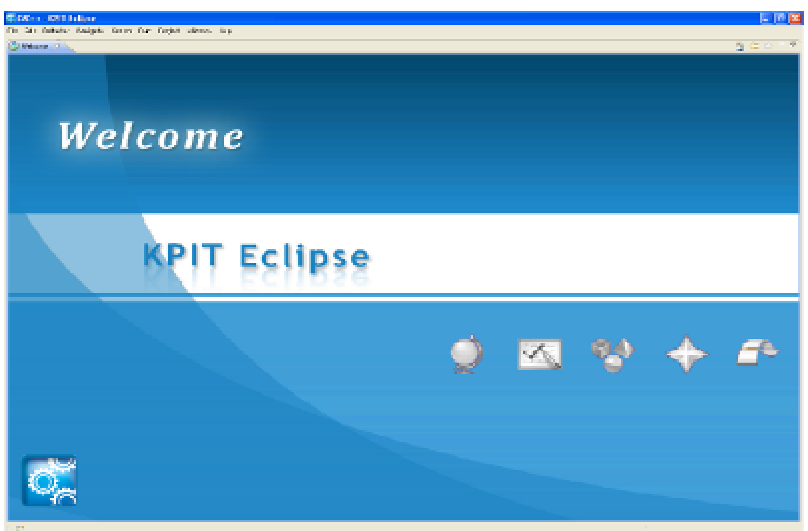
Single Integrated Development & Debugging Environment



- **For all Renesas controllers**
- **Consistent across all debug targets [Simulators, monitors,ICEs]**
- **Integrates Compiler, Debugger, Flasher, Editor and Project Management**

Eclipse support for RX600

- KPIT is our Eclipse partner
  - Already strong support for GNU compilers
- KPIT will develop build phase support for Renesas and GNU RX compilers
  - Scheduled for release end Q2 2010
- Eclipse IDE (CDT) & RX GNU will be available for download free of charge from KPIT web site



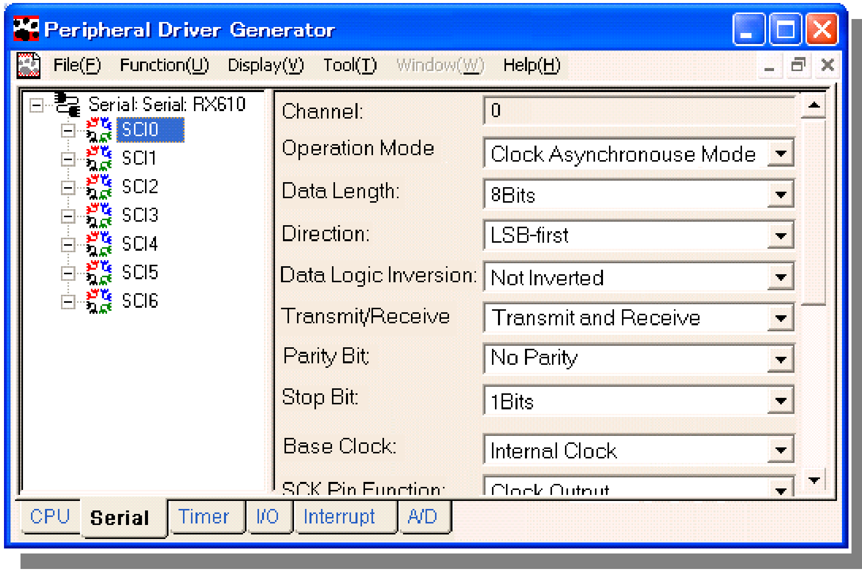
Renesas Peripheral Driver Library (RPDL)

- Designed to reduce project start up time and portability of code
- Will generate larger code than hand coded
  - Consider time to market and code reuse in the project
- Will be supplied as fully QAed binary library
- All RX sample code will be developed using RPDL
- Plan to add Peripheral Driver Generator (PDG) GUI late

```
void func(void)
{
/* Configure pin TMO0 for 500μs period, 200μs pulse width */
__CreateTMRPeriodic(0, (RAPI_TMR_8_BIT | RAPI_TMR_PERIOD | RAPI_TMR_OUTPUT_ON), 500, 200,
RAPI_NA, 0);
}
```

PDG for RX

- GUI to sit above Renesas Peripheral Driver Library (RPDL)
- Under development (Q2 2010)



Peripheral Driver Generator

```
#include “r_pdl_sci.h”
void func(void)
{
/* Configure SCI0 for asynchronous mode, 8N1, 38400 baud */
R_SCI_CreateRate(0, PDL_SCI_8N1, 38400, 1);
}
```

Renesas Starter Kit - RSK

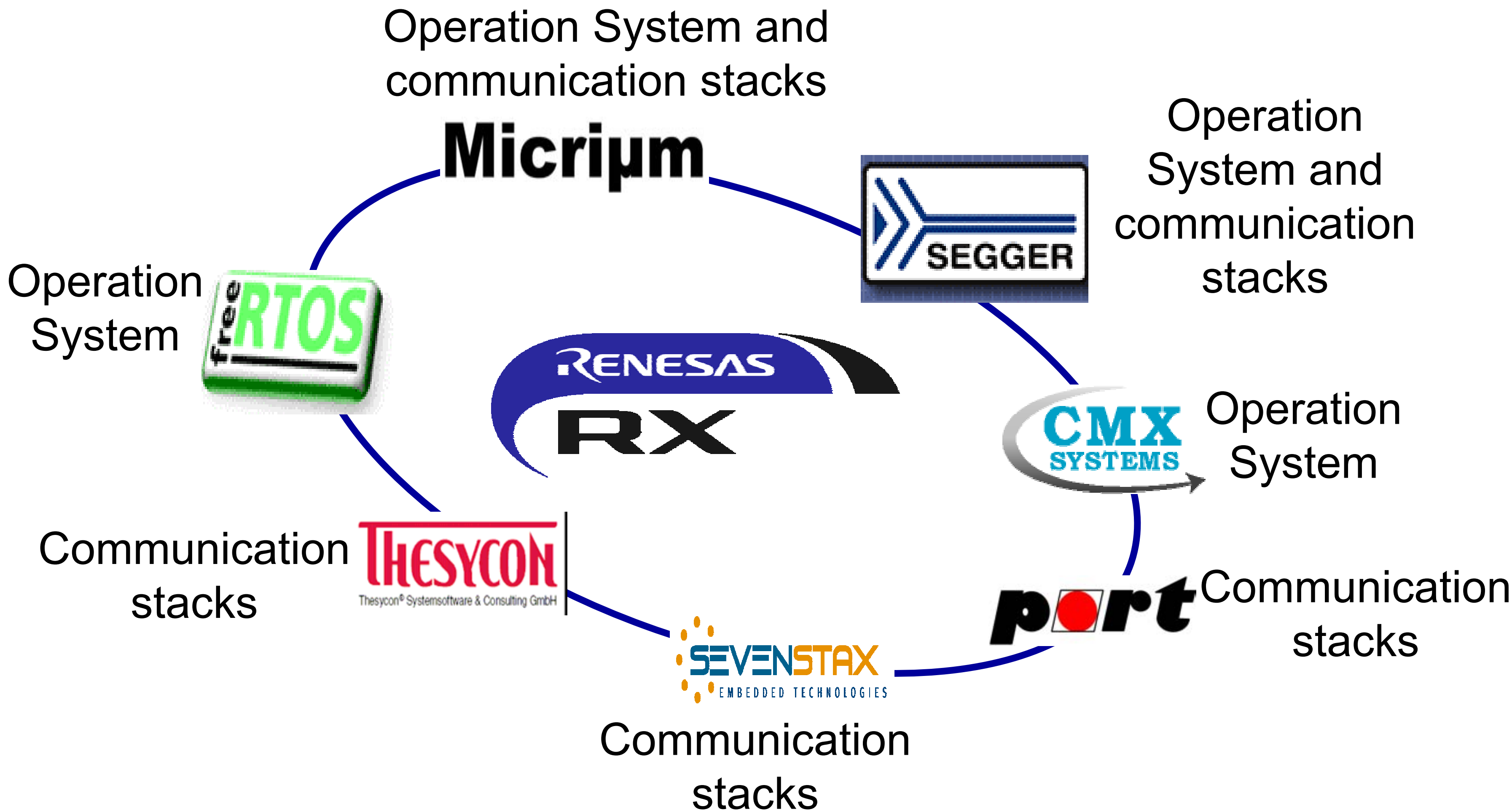
The kit includes:

- CPU board with target microcontroller
- LCD panel for user/diagnostic interaction
- E1 JTAG On Chip Debugger
- Trial Renesas C compiler and IDE
  (60 days unlimited then 128K limited)
- Tutorial session
- Sample peripheral driver code

	Schedule	Supported Devices	Order p/n
RSK RX610	**MP**	RX610	R0K556100S000BE
RSK RX62N	**Q3/2010**	RX62N, RX621	R0K5562N0S000BE
RSK RX62T	**Q3/2010**	RX62T	R0K5562T0S000BE

RX600 Third Party Infrastructure

- A wide range of excellent partners for Operation System and Communication Stacks.



Any Questions?

Thank you!

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