



Precision Analog Microcontroller 12-bit ADC and DACs, ARM7TDMI® Core

Silicon Anomaly List

ADuC702x

A. This Anomaly list describes the known bugs, anomalies, work-arounds and planned feature enhancements for the ADuC702x MicroConverter.

B. The anomalies listed, apply to all ADuC702x packaged material branded as follows:

(Sampling Material)
ADuC702xBCP H3T

C. Analog Devices Inc. is committed, through future silicon revisions to continuously improve silicon functionality. Analog Devices Inc. will use its best endeavours to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended work-arounds outlined in this document.

D. Anomaly List Contents :

Section 1: ADuC702x Functionality Issues

Revision	Date	Relevance	Silicon Status	# of Issues Reported
0.29	August 2005	All Silicon branded ADUC702xBCP H3T	Sampling	1

Section 2: ADuC702x Performance Related Issues

Revision	Date	Relevance	Silicon Status	# of Issues Reported
0.29	August 2005	All Silicon branded ADUC702xBCP H3T	Sampling	1

Section 3: ADuC702x Silicon Future Enhancements

Revision	Date	Relevance	Silicon Status	# of Issues Reported
0.29	August 2005	All Silicon branded ADUC702xBCP H3T	Sampling	0

REV. 0.29 August 2005

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Section 1: ADuC702x Functionality Issues

1. PWM SYNC INTERRUPT [er014]:

Background: The PWM block provides a synchronisation pulse that is used to synchronise to the PWM switching frequency. The PWM can be configured to generate an interrupt on this SYNC pulse.

Issue: The PWM will not produce an interrupt correctly on the SYNC pulse.

Work-Around: Output the synchronisation pulse on the SYNC pin and route it through a PLA element. The PLA can then be configured to give an interrupt on the SYNC pulse.

Related Issues: None.

Section 2: ADuC702x Performance related issues

1. EXECUTION SPEED [pr003]:

Background: The Flash/EE memory access time is 22ns. The peak performance in Thumb mode is therefore 41.78 MIPS and 20.89 MIPS in ARM mode when executing from Flash/EE memory.

Issue: The Flash/EE access time is configured to be 44ns. The maximum speed of code execution is therefore reduced to 20.89 MIPS peak (CD = 0) in Thumb mode and 10.44 MIPS peak (CD = 0) in ARM mode. This is due to the default values in the FEEMOD MMR being incorrect.

Work-Around: The FEEMOD MMR should be modified at the start of the user code to obtain the maximum performance from the Flash/EE memory, 41.78 MIPS and 20.89 MIPS peak in Thumb and ARM modes respectively. This is done by changing bit 0 in FEEMOD from it's (incorrect) default value of "1" to "0".

Related Issues: None.

Section 3: ADuC702x Silicon Future Enhancements

Errata Sheet History

Issue	REF	Status
Section 1: ADuC702x Functionality Issues		
EXTERNAL REFERENCE	[ER001]	FIXED
ADC WRAP AROUND	[ER002]	FIXED
FLASH/EE CONTROLLER	[ER003]	FIXED
CODE EXECUTION, 1KB BOUNDARY ISSUE	[ER004]	FIXED
CLOCKING SYSTEM	[ER005]	FIXED
WAKE-UP TIMER OPERATION	[ER006]	FIXED
I2C TRANSMIT FIFO FLUSH OPERATION	[ER007]	FIXED
USE OF I2C IN MASTER MODE	[ER008]	FIXED
BLOCK INTERCONNECTION IN PLA PERIPHERAL	[ER009]	FIXED
BAUD RATE GENERATION	[ER010]	FIXED
TEMPERATURE SENSOR OPERATION	[ER011]	FIXED
PLA CLOCK SOURCE PINS	[ER012]	FIXED
ADC POWER-UP TIME	[ER013]	FEATURE
PWM SYNC INTERRUPT	[ER014]	OPEN
WATCHDOG TIMER OPERATION	[ER015]	FIXED
EXTERNAL MEMORY BUS OPERATION	[ER016]	FIXED
Section 2: ADuC702x Performance Related Issues		
ADC LINEARITY	[PR001]	FIXED
DAC GAIN ERROR	[PR002]	FIXED
EXECUTION SPEED	[PR003]	OPEN
FLASH RETENTION SPECIFICATION	[PR004]	FIXED
Section 3: ADuC702x Silicon Future Enhancements		
I ² C ADDRESS MATCHING	[FE001]	FIXED
I ² C START AND STOP CONDITION IDENTIFICATION	[FE002]	FIXED
EXTERNAL CLOCK INPUT PIN	[FE003]	FIXED