X-board™ <861>

X-board™ <861> User's Guide

Document Revision 2.0

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CONTENTS

1. USER INFORMATION

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1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules technical support, please consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

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2. INTRODUCTION

2.1 *X-board™ Benefits*

The X-board™ modules of Kontron Embedded Modules GmbH are very compact (49mm x 68mm x 6mm) and highly integrated computers. All X-board™ modules have a standardized form factor and a standardized connector (DDR-SODIMM Memory Connector) that carries a specified set of signals. This standardization allows designers to create a single system "baseboard" which can accept a variety of present and future X-board™ modules.

X-board™ modules include common personal computer (PC) peripheral functions such as serial ports, Ethernet, IDE, USB, etc.

The baseboard designer can optimize exactly how each of these functions is physically implemented. Connectors can be placed precisely where they are needed for the application, on a baseboard designed to optimally fit the system configuration and layout.

Legacy devices are omitted to reach a maximum in compactness and size.

Peripheral PCI or LPC devices can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard, using the computer as one "plug in" component, simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design may be used with a range of X-board™ modules. This flexibility can be used to differentiate products at various price/performance points, or to design "future proof" systems that have a built-in upgrade path. The modularity of an X-board™ solution also insures against obsolescence as computer technology continues to evolve. A properly designed X-board™ baseboard can be used with several successive generations of X-board™ modules.

An X-board™ baseboard design thus has many of the advantages of a custom computer board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

2.2 *X-board™ Documentation*

This manual is intended as one of three principal references for an X-board™ design.

- The X-board™ specification defines the X-board™ module form factor, pinout and signals. It is suggested that this be read first.
- The design guide is intended as a general guide for baseboard design, with a focus on maximum flexibility in order to accommodate a wide range of X-board™ modules.
- Finally, the technical manuals for specific X-board™ modules document the specifications and features of each individual X-board™ module.

3. SPECIFICATIONS

3.1 *Functional Specifications*

- **Processor: National Semiconductor SC1200**
- **Bus: 33MHz bus clock**
- **Chipset: National Semiconductor SC1200**
- **Cache: 16KB integrated cache**
- **Onboard Memory: SDRAM with 16/32/128MB**
- ***Two Serial Ports (COM1 and COM2)**
  - COM 1 Transistor-to-transistor (TTL) signals only
  - COM 2 (TTL) only two wires available (RXD, TXD)

*This serial port configuration is only available from Product rev. X16 and BIOS rev. XBD1R112.ROM

- **Enhanced Intelligent Drive Electronics (EIDE): One Peripheral Component Interconnect (PCI) Bus Master, IDE ports (up to two devices) support:**
  - Programmed Input/Output (PIO) modes up to Mode 4 timing
  - Optional onboard IDE flash device with either 16/32/64/128MB
- **Universal Serial Bus (USB)**
  - Three USB 1.1 ports (OHCI)
  - USB legacy keyboard support
  - USB floppy-boot support
- **Low Pin Count Bus (LPC)**
- **Onboard Ethernet: · Intel 82551ER PCI single chip**
  - 10BASE-T/100BASE-T LAN
  - Fast Ethernet NIC controller
- **Onboard video graphics array (VGA): Integrated in National SC1200**
  - 2D graphics accelerator and display controller
  - Cathode ray tube (CRT) and liquid-crystal display (LCD) panel support: digital signals (JIDI)
  - Resolution up to 1280 x 1024 x 8bpp (CRT)
  - Resolution up to 1024 x 768 x 16bpp (CRT)
  - Up to 4MB video RAM (UMA)
  - TV Output (only available on BIOS revisions XBD1R113.rom and later)
- **Audio: Integrated AC'97 Interface on National SC1200**
  - AC'97 Interface to connect an AC'97 codec
- **BIOS: Insyde, 512KB Flash BIOS**
  - BIOS support for external LPC super I/O (PS/2, COM3, COM4, LPT, and Floppy)
- **NV-EEPROM for CMOS setup**

- **Watchdog timer (WDT)**
- **Real-time clock (requires an external battery)**

3.2 *Mechanical Specifications*

3.2.1. Dimensions

- 49.0 mm x 68.0 mm
- Height approx. 6 mm

3.3 *Electrical Specifications*

3.3.1. Supply Voltage

- 3.3 VDC +/- 5%

3.3.2. Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

3.3.3. Supply Current (typical, DOS prompt)

- 900 mA

It was measured with a board with 128 MB RAM and 128 MB onboard IDE flash connected in a backplane without additional power consuming components.

3.3.4. CMOS Battery Power Consumption

RTC	Voltage	typical Current	max. Current
@ T_C=25 °C	2.4 V	6.3 µA	
	3.0 V	7.5 µA	50 µA

Data source: AMD Geode SC1200 datasheet revision 7.0

3.3.5. APM 1.2 Support

The X-board<861> supports APM 1.2 and has a standby and suspend state. Additionally during idle mode the board is in a low power state. This reduces the power tremendously when using operating systems that are able to switch the processor to idle mode (not DOS).

The following table shows the current on the 3.3V line that powers the X-board<861>.

Status	Current
Full On	890 mA
Idle	530 mA
Standby	480 mA
Suspend	390 mA

The measurements were done using a board with 32MB flash and 32MB RAM on a backplane without additional power draining components.

The board was booted from a HDD with RedHat Linux including the APM Kernel.

The Idle state was measured in console mode at the prompt.

Resume is controlled by interrupts activated in the BIOS setup. This does not work in Windows 98 with PS/2 Mouse/Keyboard and with USB Mouse/Keyboard because Windows 98 deactivates the driver for PS/2 and USB during standby and suspend, which does not allow a resume. In Linux resume with USB Mouse/Keyboard is not possible.

3.4 *Environmental Specifications*

3.4.1. Temperature

- Operating: 0 to +65°C
- Non operating: -10 to +85°C

Note: The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification. For more information about cooling solutions please contact Kontron Embedded Modules.

3.4.2. Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

4. CPU, CHIPSET, AND SUPER I/O

4.1 *CPU and Chipset*

The central processing unit (CPU) and the Chipset (North and South bridge) consists of a National Semiconductor SC1200 and is available at a speed of 266MHz. Features include:

- Support for Intel's MMX instruction set extension for acceleration of multimedia applications (one pipeline)
- 16KB unified L1 cache
- PCI host controller
- 2D graphics accelerator and display controller
- SDRAM interface tightly coupled to CPU core and graphics subsystem for maximum efficiency
- Provides 16-bit Xpress AUDIO subsystem, AC'97 Interface
- 3.3V PCI bus compatible
- PCI 2.1 compliant
- PCI master for audio I/O and IDE controllers
- Two 8259A-equivalent interrupt controllers
- 8254-equivalent timer
- Two 8237-equivalent DMA controllers
- Boot ROM chip select
- One controller with support for up to two IDE devices
- Independent timing for master and slave devices
- AC97 codec interface (Specification Revision 2.0 compliant interface)
- Three independent USB interfaces
    - Open Host Controller Interface (OpenHCI) specification compliant
    - Second-generation core design

5. SYSTEM MEMORY

5.1 SDRAM

The *X-board<861>* uses onboard-unbuffered Synchronous Dynamic Random Access Memory (SDRAM) sizes of 16, 32 or 128MB.

6. INTERFACES

6.1 *PCI Bus*

The implementation of this subsystem complies with the *X-board™* Specification. Implementation information is provided in the *X-board™ Design Guide*. Refer to the documentation for additional information.

6.2 *LPC Bus*

The implementation of this subsystem complies with the *X-board™* Specification. Implementation information is provided in the *X-board™ Design Guide*. Refer to the documentation for additional information.

The LPC Bus is the subtractive decoding agent in this system, i.e. all I/O and memory accesses, which don't belong to onboard RAM, internal chipset devices, onboard Super I/O or PCI devices, are linked to the LPC bus.

Note * If the LPC interface is not used on the customers backplane, then the signals LAD[0..3] and LDRQ# have to be connected together and pulled-up to 3.3V with an 15kΩ resistor.

6.3 *IDE Ports*

The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.3.1. Configuration

The IDE host adapter is a PCI bus device. BIOS configures it during PCI device configuration. You can disable it by using the BIOS setup. Resources used by the IDE host adapter are compatible with the PC/AT.

6.4 *Serial ATA Signals*

Serial ATA is not supported by X-board<861>

6.5 *Serial Ports (1 and 2)*

The implementation of the serial-communication interface is restricted. COM1 supports TxD, RxD, #RTS, #DTR, #CTS, #DCD, #DSR, #RI, and COM2 only supports RXD and TXD. Implementation information is provided in the *X-board™ Design Guide*. Refer to the documentation for additional information.

6.5.1. Configuration

The serial-communication interface uses I/O and IRQ resources. The resources are allocated by BIOS during POST configuration and are set to be compatible with common PC/AT settings. Use the BIOS setup to change some parameters that relate to the serial-communication interface.

6.6 *USB*

Three OHCI-type USB host controllers are on the National SC1200 single chip processor. The USB controllers comply with Version 1.1 of the USB standard. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.6.1. Configuration

The USB controllers are PCI bus devices. BIOS allocates required system resources during configuration of the PCI bus.

6.7 *Ethernet*

The 82551ER is a fully integrated, cost-effective 10BASE-T/100BASE-TX LAN solution. It is designed for low-power use and high-performance processes. It is a 3.3V device with 5V tolerance and supports 3.3V and 5V signaling.

6.7.1. Configuration

The Ethernet interface is a PCI device. The BIOS setup automatically configures it.

6.8 *AC'97 Codec Interface*

The sound function on the *X-board<861>* board comes from the AC'97 interface of the National Semiconductor's SC1200. An external Codec must be connected on the baseboard to use the audio functions. Please look at the implementation information provided in the *X-board™ Design Guide*.

6.8.1. Configuration

The audio controller is a PCI bus device. BIOS allocates required system resources during configuration of the PCI device.

6.9 *VGA Output*

The National SC1200 includes the display subsystem:

- Video accelerator
  - Buffers and formats input YUV video data from processor

- 8-bit interface
- X & Y scaler with bilinear filter
- Color space converter (YUV to RGB)

➤ Display Interface

- Integrated RGB video DACs
- VESA DDC2B/DPMS support
- Flat-panel interface
- Brightness and contrast control

➤ Supported Resolutions for CRT

- Up to 1024 x 768 x 16bpp (64k colors)
- 1280 x 1024 x 8bpp (256 colors)

➤ Supported Resolutions for LCD (JIDI)

- With LVDS transceiver on the backplane: up to 1024 x 768 x 16bpp (64k colors)
- Only TTL signals: up to 640 x 480 x 16bpp (64k colors)

➤ Simultaneous Resolution Mode (CRT and LCD)

- Up to 800 x 600 x 16bpp

➤ TV Output Support

- PAL and NTSC composite 640 x 480 (only available on BIOS revisions XBD1R113.rom and later)

6.9.1. Configuration

The graphics controller requires the following resources:

➤ An IRQ

➤ Several I/O addresses

➤ Memory-address blocks in high memory

BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

6.10 *Digital Flat Panel Interface (JIDI)*

Optionally, the *X-board<861>* supports the JUMPtec Intelligent Digital Interface (JIDI). It provides the possibility to store controller specific panel configuration data in an external eeprom. It additionally allows to store the panel ID regarding the JILI3 specification.

As a special feature also this panel ID can be directly keyed in the BIOS setup. Therefore an external EEPROM on the panel interface is no longer necessary.

Please contact Kontron Embedded Modules Technical Support for more information.

6.11 *Television Output*

The *X-board<861>* supports television output (only available on BIOS revisions XBD1R113.rom and later). Standard PAL and NTSC composite output supported.

6.12 SMB/I2C BUS

The X-board<861> provides only the I²C bus on that interface.

6.13 Power Control

6.13.1. Power Good / Reset Input

The *X-board<861>* provides an external input for a power good signal or a manual reset pushbutton. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.14 Power Management

6.14.1. ATX PS Control

The *X-board* <861> can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.15 Miscellaneous Circuits

6.15.1. Battery

The implementation of the battery input complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.16 Watchdog Timer

This feature is implemented in National SC1200. You can configure the Watchdog Timer (WDT) from the BIOS setup to start after a set amount of time following power-on boot. The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

6.16.1. Configuration

You can program the initial delay period for the WDT in ranges from 000000h * 0,256 sec to 07FFFh * 0,256 Sec.

You can also program the timeout period for the WDT in ranges from 000000h * 0,256 sec to 07FFFh * 0,256 Sec.

Contact Kontron Embedded Modules for information about programming and operating the WDT.

6.16.2. Strap Pins

- AC97_Sync (Pin 11), 1k5 to GND
- AC97_DOUT (Pin 5), 1k5 to 3.3V supply
- COM1_TxD (Pin 51), 1k5 to GND
- COM2_TxD (Pin 65), 1k5 to 3.3V supply
- GNT1# (Pin 181), 1k5 to GND
- GNT0# (Pin 185), 1k5 to GND

During the power-up sequence of the X-board <861> several signals are read that set up the state of the SC1200/SC1201 (chipset). These particular signals are usually multiplexed with other functions that result in outputs after the power-up sequence is completed. While powering up, the X-board <861> has to read the current state of the signals and yet the internal PU or PD resistors don't necessarily guarantee that the correct state will be read. For this reason it is essential that an external PU or PD resistor with a value of 1.5 KΩ be placed on the signals listed above. Kontron Embedded Modules has implemented this in their X-board <861> design. The X-board <861> user must ensure that they do not alter the signals mentioned above in any way. The value of the resistor is extremely important so that the proper state is read during the power-up sequence. If the ball produces an incorrect reading during power-up then the X-board <861> may default to a state that causes it to function improperly, which could result in undesired behavior such as an application failure.

This table shows the values that must be maintained when using an external PU or PD.
(extracted from National/AMD chipset datasheets page 378)

Symbol	Parameter	Min	Max	Unit	Comments
V_{IH}	Input High Voltage	$0.6V_{IO}$	$V_{IO}+0.5$	V	
V_{IL}	Input Low Voltage		$0.3V_{IO}$	V	
I_{IL}	Input Leakage Current		36	µA	During Reset $V_{IN} = V_{IO}$
			-10	µA	$V_{IN} = V_{SS}$

7. LIMITATIONS

7.1 PCI

GNT1#/REQ1# are used by Ethernet, therefore not available for external PCI devices.

7.2 Watchdog

The Watchdog only allows RESET, no NMI operation.

7.3 USB boot

USB CD-ROM and USB hard disk boot support. Access to USB hard disk is not possible if the USB hard disk is not the boot device. This will also be implemented later.

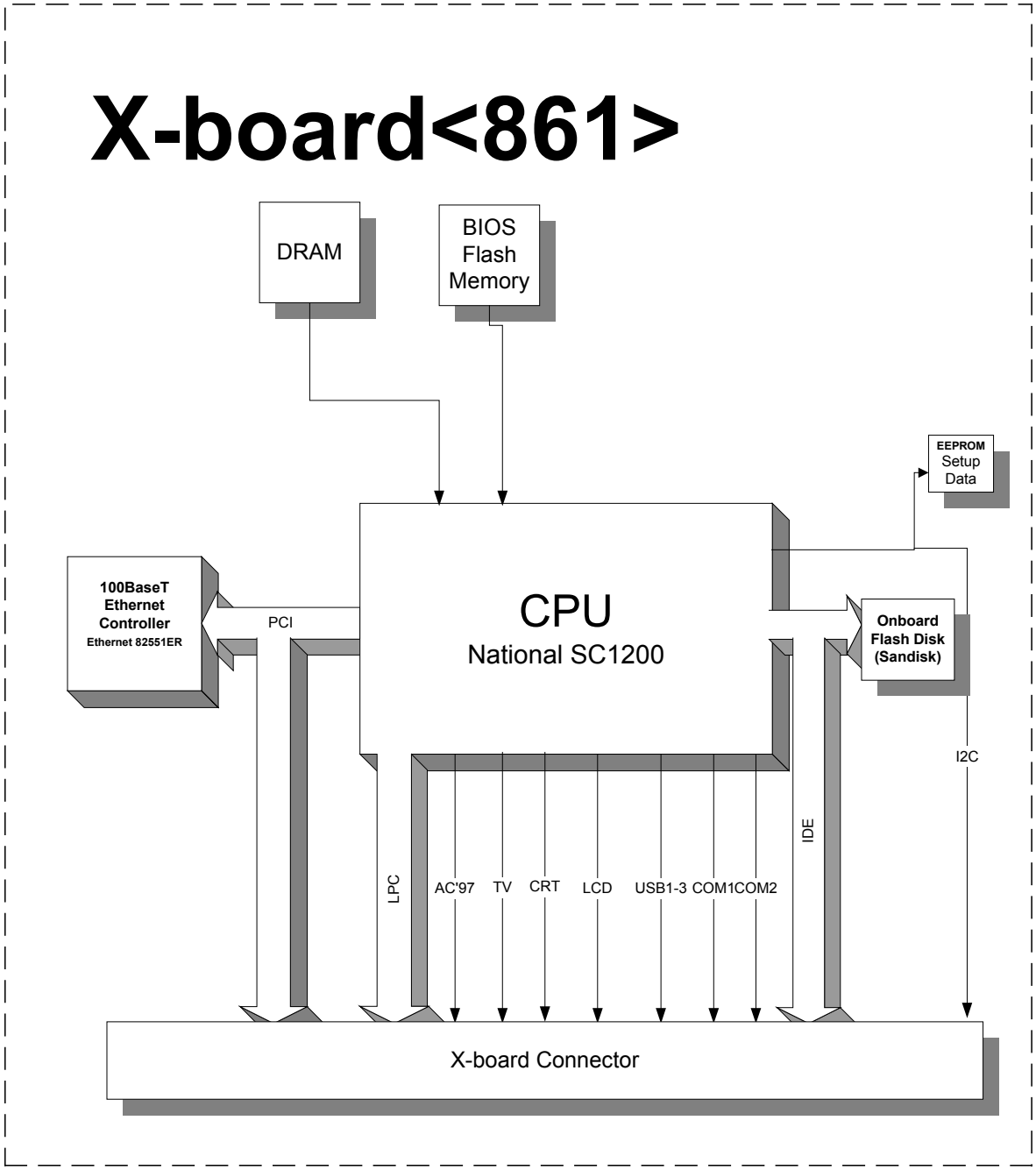
7.4 Keyboard / Mouse usage

You can either use a USB mouse and keyboard, or a PS/2 mouse and keyboard. Once a USB mouse or USB keyboard is plugged in, PS/2 devices are disabled.

7.5 I²C Bus

The I²C bus is also used for JILI/JIDI devices, therefore there may be additional devices (JILI Data EEPROM, Backlight DAC) reducing the number of available addresses. Please refer to the JILI manual to find out which addresses may not be available.

8. APPENDIX A: BLOCK DIAGRAM



9. APPENDIX B: SYSTEM RESOURCES

9.1 Interrupt Request (IRQ) Lines

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	LPC (Keyboard Controller)	No	
2	Cascade	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1)
6	LPC (Floppy Controller)	No	Note (1,2)
7	LPC (LPT)	No	Note (1,2)
8	RTC	No	
9	PCI (default for INT A)	Yes	
10	PCI (default for INT B)	Yes	Note (3)
11	PCI (default for INT D)	Yes	Note (3)
12	LPC (PS/2 Mouse)	No	Note (2)
13	FPU	No	
14	IDE0	No	Note (1)
15	PCI; LPC	Yes	

Notes: [1] If the "Used For" device is disabled in setup or not connected on the backplane, the corresponding interrupt is available for other devices.
[2] In use if the baseboard is equipped with I/O controller PC87365.
[3] If not used for PCI it is routed to LPC (available for COM3 and COM4)

9.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0	LPC	Yes	
1	Sound 8-bit	No	Note (1)
2	FDC	No	Note (1)
3	LPT	No	Unavailable if LPT used in ECP mode.
4	Cascade	No	
5	Sound 16-bit	No	Note (1)
6		Yes	
7		Yes	

Note: [1] If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

9.3 *Memory Area*

Upper Memory	Used for	Available	Comment
C0000h – C8000h	VGA BIOS	No	
C8000h – CFFFFh	USB-boot ROM	No	
D0000h – DFFFFh	LPC or UMB	Yes	LPC bus or shadow RAM
E0000h - FFFFFh	System BIOS	No	

All memory accesses above TOP_OF_MEMORY (=installed RAM), if not explicitly noted below, are available for PCI or LPC bus devices (PCI positive decoding takes precedence).

Details/Special Devices: The BIOS will map all PCI memory areas above 40000000h; thus memory from TOP_OF_RAM to 40000000h (1GB) will be exclusively available for LPC devices.

9.4 *I/O Address Map*

The I/O-port addresses of the *X-board<861>* are functionally identical with a standard PC/AT.

PC/AT Standard I/O addresses should be assumed to be used.

LPC devices should not try to map (use) I/O addresses below 400h, unless it is an LPC Super I/O, which implement legacy PC hardware like COM, LPT, Floppy or Keyboard/Mouse.

The following I/O ports >400h are used by the chipset and onboard resources:

I/O Address	Used for	Available	Comment
0480h - 048Fh	chipset internal	No	
04D0h - 04D1h	Interrupt sensitivity configuration registers (standardized)	No	
0860h - 086Fh	chipset internal	No	
0CF0h - 0CFFh	PCI configuration registers	No	
5000h - 500Fh	chipset internal	No	
6000h - 60FFh	chipset internal	No	
6200h - 623Fh	chipset internal	No	
6400h - 643Fh	chipset internal	No	
6600h - 663Fh	chipset internal	No	
9000h - 90FFh	chipset internal	No	
9C00h - 9CFFh	chipset internal	No	

9.5 *Peripheral Component Interconnect (PCI) Devices*

PCI Device	PCI Interrupt	Comment
Sound	INTC (internal)	Chipset integrated, no REQ/GNT pairs used
Ethernet	INTA	Use REQ1/GNT1 pair
Graphic	no	No use of an internal REQ/GNT pair.
USB Controller	no	No use of an internal REQ/GNT pair

You can use only REQ0/GNT0 pair for external PCI devices. In the *X-board™ Design Guide* you find additional information about how to expand these pairs by using certain devices on the backplane

Only INTA and INTB are externally available.

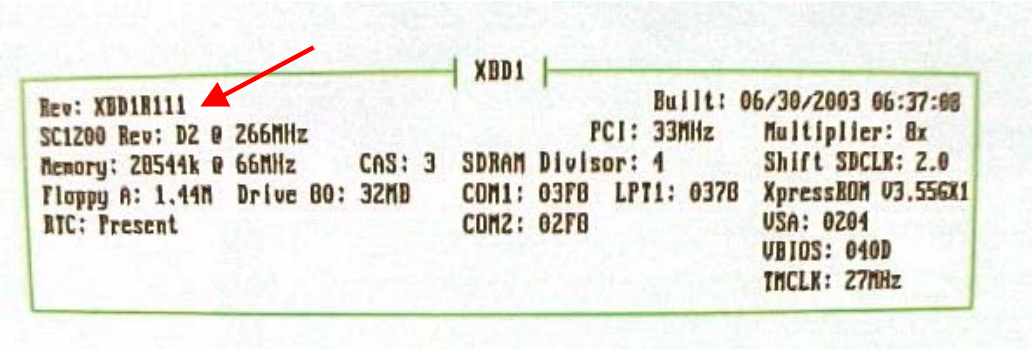
10. APPENDIX C: BIOS OPERATION

The Module is equipped with an Insyde XpressROM™ BIOS, which is located in an onboard Flash EEPROM.

You can update the BIOS using a Flash utility.

10.1 *Determining the BIOS Version*

To determine the BIOS version, the summery screen in the BIOS setup must be activated. The information is located in the summery screen (marked here with a red arrow):



10.2 *Setup Guide*

The Insyde BIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and to turn features on or off.

The BIOS setup menus documented in this section represent those found in most models of the X-board<861>. The BIOS Setup for specific models can differ slightly.

10.2.1. Start BIOS Setup Utility

To start the setup utility, press <**F1**> during boot up when the following string appears.

```
Press F1 to enter Setup
```

The Main Menu then appears.

10.2.2. BIOS Setup Navigation

Navigation through the setup can be done either by using the cursor keys ← or →and ↑ or ↓, or by pressing the character keys that are shown in front of every menu item.

A menu item is either a field for selecting and changing an entry or a submenu. To change an entry, or to jump into a submenu, press the enter key <ENTER>.

To jump back from a submenu press the <ESC> key.

In the option column, **bold** shows the BIOS default values.

10.3 *Main Menu*

Character	Feature	Option	Description
A	Time	HH:MM:SS	Set the system time
B	Date	MM/DD/YYYY	Set the system date
C	Motherboard Device Configuration		Submenu for Device Configuration
D*	Memory Optimization		Submenu for memory timing control
F	Power Management		Submenu for Power Management
H	Miscellaneous Configuration		Submenu for Miscellaneous Configuration
L	Load Defaults		Loads the setup defaults
S	Saves Values Without Exit		Save all values and stay in Setup Utility
Q	Exit Without Save		Quit Setup Utility without saving the changes
X	Save Values and Exit		Saves all changes and exit Setup Utility

Note: * This feature is only available on X-board <861> modules that have BIOS revision XBD1R112.rom or later.

10.3.1. Motherboard Device Configuration Submenu

Character	Feature	Description
A	Drive Configuration	Submenu for Drive Configuration
B	Onboard Super I/O Configuration	Submenu for Super I/O Configuration
C*	LPC Bus & LPC Super I/O Configuration	Submenu for LPC Bus & LPC Super I/O Configuration
D**	TV Output Configuration	Submenu for TV Output
E	Legacy Audio Configuration	Submenu for Audio Configuration
F	Video and Flat Panel Configuration	Submenu for Video and Flat Panel Configuration
G	PCI Configuration	Submenu for PCI Configuration
R	Return to Main Page	Returns to Main Menu

Note: * This feature is only available on X-board <861> modules that have BIOS revision XBD1R112.rom or later.
**This feature is only available on X-board <861> modules that have BIOS revision XBD1R113.rom or later

Drive Configuration

Feature	Option	Description
IDE Configuration		
Chipset IDE Channel	**Primary** Disabled	Switch the single IDE channel ON and OFF
Max PIO mode for Drive 1	**Auto** PIO0 PIO1 PIO2 PIO3 PIO4	Switches on the maximum transfer mode of the IDE Drive 1
Max PIO mode for Drive 2	**Auto** PIO0 PIO1 PIO2 PIO3 PIO4	Switches on the maximum transfer mode of the IDE Drive 2
Boot ROM Configuration		
CD-ROM Boot-ROM	**Enabled** Disabled	Enable and Disable the possibility to boot from IDE CD-

		ROM devices
USB Mass Storage Boot-ROM	**Enabled** Disabled	Enable and Disable the possibility to boot from USB Mass Storage devices
PXE Lanboot Option ROM	Enabled Flag Controlled **Disabled**	Enable and Disable the possibility to boot from LAN
Boot Order Configuration		
1.	**Floppy Disk** Hard Drive #1 Hard Drive #2 USB Mass Storage IDE-CDROM Drive None Network Boot	Selects the 1st boot device
2.	Floppy Disk Hard Drive #1 Hard Drive #2 **USB Mass Storage** IDE-CDROM Drive None Network Boot	Selects the 2nd boot device
3.	Floppy Disk Hard Drive #1 Hard Drive #2 USB Mass Storage **IDE-CDROM Drive** None Network Boot	Selects the 3rd boot device
4.	Floppy Disk **Hard Drive #1** Hard Drive #2 USB Mass Storage IDE-CDROM Drive None Network Boot	Selects the 4th boot device
5.	Floppy Disk Hard Drive #1 **Hard Drive #2** USB Mass Storage IDE-CDROM Drive None Network Boot	Selects the 5th boot device
6.	Floppy Disk Hard Drive #1 Hard Drive #2 USB Mass Storage IDE-CDROM Drive None **Network Boot**	Selects the 6th boot device
5.	Floppy Disk Hard Drive #1 Hard Drive #2 USB Mass Storage IDE-CDROM Drive None **Network Boot**	Selects the 7th boot device

Onboard Super I/O Configuration

Feature	Option	Description
Serial Port A	**0x3f8 IRQ 4** 0x2f8 IRQ 3 0x3e8 IRQ 4 0x2e8 IRQ 3 Disabled	Selects the resources of 1st onboard serial port
Serial Port B	0x3f8 IRQ 4	Selects the resources of 2nd onboard serial

	0x2f8 IRQ 3 0x3e8 IRQ 4 0x2e8 IRQ 3 Disabled	port

LPC Bus & LPC Super I/O Configuration

Feature	Option	Description
LPC Bus*	**Enabled** Disabled	Enable or disable the complete LPC bus (including LPC Super I/O).
Serial Port 1	0x3f8 IRQ 4 0x2f8 IRQ 3 0x3e8 IRQ 4 0x2e8 IRQ 3 **Disabled**	Selects the resources of 1st LPC serial port
Serial Port 2	0x3f8 IRQ 4 0x2f8 IRQ 3 0x3e8 IRQ 4 0x2e8 IRQ 3 **Disabled**	Selects the resources of 2nd LPC serial port
Parallel Port	**0x378** 0x278 0x3bc Disabled	Selects the resources of 2nd onboard serial port
Mode	**Compatible** PS/2 Bidirectional EPP 1.7 EPP 1.9	Sets the Mode for the Parallel Port
IRQ	**IRQ 7** Disabled IRQ 5	Sets the IRQ for the Parallel Port
DMA	**None** Channel 3 Channel 1	Sets the DMA Channel for the Parallel Port

Note: * This feature is only available on X-board <861> modules that have BIOS revision XBD1R112.rom or later.

TV Output Configuration

Feature	Option	Description
TV Output	**Disabled** Composite	Enables the Composite output
Format	**PAL** NTSC	Selects format for TV Output
Mode	**640x480**	Only resolution available
Horizontal Position	0-255	Allows you to center image on TV screen. Each increment moves the image 1 character (8 pixels) to the right.

Note: This feature is only available on X-board <861> modules that have BIOS revision XBD1R113.rom or later.

Legacy Audio Configuration

Feature	Option	Description
Audio Enable	**Disabled** Enabled	Enables the Legacy Audio Interface
Audio Base	**0x220** 0x240 0x260 0x280	Selects the I/O Address of the Audio Interface
Audio IRQ	**IRQ 5** IRQ 7 IRQ 9 IRQ 10	Selects the IRQ of the Audio Interface

	Disabled	
Audio 8-bit DMA	**Channel 1** Channel 3 Channel 5 Disabled Channel 0	Sets the DMA Channel for 8-bit audio transfers
Audio 16-bit DMA	Channel 1 Channel 3 **Channel 5** Disabled Channel 0	Sets the DMA Channel for 16-bit audio transfers

Video and Flat Panel Configuration

Feature	Option	Description
Video Memory	**4 MB** None 1,0 MB 1,5 MB 2,0 MB 2,5 MB 3,0 MB 3,5 MB	Selects the size of Video Memory. This value is reducing the RAM
Flat Panel Mode	**Enabled** Disabled	Enables and disables the flat panel interface
Flat Panel Type	**Auto Detect** Use Panel ID 640x480 800x600 1024x768	Switches between usage of I²C EEPROM, fixed Panel ID in setup or standard settings for common panels
Panel ID	00000	Flat panel ID to be used without EEPROM directly to set in the setup
Backlight Configuration		
Brightness Control	**Disabled** Enabled	Enable and disable the Control of DACs on the I²C bus to control the brightness via JIDA
Initial Brightness	**Last Value** 0% (OFF) 10% … 90% 100% (Full ON)	Select the initial brightness of the backlight, if it is controlled via JIDA on the I²C bus
Contrast Configuration		
Contrast Control	**Disabled** Enabled	Enables or disables the Control of DACs on the I²C bus to control the contrast via JIDA
Initial Contrast	**Last Value** 0% (OFF) 10% … 90% 100% (Full ON)	Selects the initial contrast of the STN panel, if it is controlled via JIDA on the I²C bus

PCI Configuration

Feature	Option	Description
PCI INTA#	**IRQ 9** IRQ 10 IRQ 11 IRQ 12 IRQ 14 IRQ 15 Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6	Fixes an interrupt to PCI INT line A

	IRQ 7	
PCI INTB#	IRQ 9 **IRQ 10** IRQ 11 IRQ 12 IRQ 14 IRQ 15 Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7	Fixes an interrupt to PCI INT line B
PCI INTC#	IRQ 9 IRQ 10 IRQ 11 IRQ 12 IRQ 14 IRQ 15 Disabled IRQ 3 IRQ 4 **IRQ 5** IRQ 6 IRQ 7	Fixes an interrupt to PCI INT line C (exclusively used by chipset integrated audio controller).
PCI INTD#	IRQ 9 IRQ 10 **IRQ 11** IRQ 12 IRQ 14 IRQ 15 Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7	Fixes an interrupt to PCI INT line D (exclusively used by chipset integrated audio controller).

10.3.2. Memory Optimization

Feature	Option	Description
Memory Optimization*	**Auto** Manual	Select memory timing auto configuration or manual selection.
SDRAM Bus Frequency*	106MHz 88MHz 75MHz **66MHz** 60MHz	Select base SDRAM bus clock.
CAS latency*	2 Clk **3 Clk** 4 Clk 5 Clk 6 Clk 7 Clk	Select CAS latency.
tRC*	2 Clk 3 Clk 4 Clk 5 Clk 6 Clk **7 Clk** 8 Clk 9 Clk 10 Clk 11 Clk 12 Clk 13 Clk 14 Clk	For Kontron customization only. Do not change.

	15 Clk 16 Clk	
tRAS*	2 Clk 3 Clk 4 Clk **5 Clk** 6 Clk 7 Clk 8 Clk 9 Clk 10 Clk 11 Clk 12 Clk 13 Clk 14 Clk 15 Clk 16 Clk	For Kontron customization only. Do not change.
tRP*	**2 Clk** 3 Clk 4 Clk 5 Clk 6 Clk 7 Clk	For Kontron customization only. Do not change.
tRCD*	2 Clk **3** Clk 4 Clk 5 Clk 6 Clk 7 Clk	For Kontron customization only. Do not change.
tRRD*	0...7 **1**	For Kontron customization only. Do not change.
tDPL*	**2 Clk** 3 Clk 4 Clk 5 Clk 6 Clk 7 Clk	For Kontron customization only. Do not change.
Cache Mode*	**Write-Back** Write-Through	Select desired L1 cache mode.

Note: * This feature is only available on X-board <861> modules that have BIOS revision XBD1R112.rom or later.

10.3.3. Power Management

Feature	Option	Description
Power Management Configuration		
Power Management Mode	**Legacy & APM** Disabled Legacy	Selects the Power Management Mode
Wakup Mask Configuration		
Wakeup Mask PIC1	**0x12**	Selects the Interrupts 0-7 by Hexadecimal no. as wakeup event
Wakeup Mask PIC2	**0x10**	Selects the Interrupts 8-15 by Hexadecimal no. as wakeup event
Timeout Configuration		
Video Timeout	**Disabled** 1 Second 5 Seconds 10 Seconds 15 Seconds 30 Seconds 45 Seconds	Time till the Video is switched off

	1 Minute 5 Minutes 10 Minutes 15 Minutes 30 Minutes 45 Minutes 60 Minutes 90 Minutes 120 Minutes	
Standby Timeout	See Video Timeout	Time till standby mode
Suspend Timeout	See Video Timeout	Time till suspend mode
Harddisk Timeout	See Video Timeout	Time till HDD is switched off

10.3.4. Miscellaneous Configuration

Feature	Option	Description
Splash Screen Configuration		
Splash Screen	Enabled **Disabled**	Enables or disables the splash screen during boot (boot logo)
Clear Splash Screen	Enabled **Disabled**	Enables or disables clearing of splash screen after display
Splash Screen Timeout	**00000**	Time until splash screen times out. Set in milliseconds
Summary Screen Configuration		
Summary Screen	**Enabled** Disabled	Enables or disables the summary screen
Summary Screen Timeout	**00100**	Time until summary screen times out in milliseconds
Watchdog Configuration		
Watchdog	**Disabled** Reset	Sets the watchdog mode
Watchdog Delay	**10 Seconds** 30 Seconds 1 Minute 2 Minutes 5 Minutes 10 Minutes 15 Minutes 30 Minutes	The watchdog will only start to count down after the given delay
Watchdog Timeout	**10 Seconds** 30 Seconds 1 Minute 2 Minutes 5 Minutes 10 Minutes 15 Minutes 30 Minutes	The watchdog must be triggered within this time interval
Legacy USB Configuration	**Enabled** Disabled During Post	Control USB legacy support
Customer ROM	**Disabled** Enabled Flag Controlled	Configure customer option ROM start

11. APPENDIX D: X-BOARD CONNECTOR PINOUTS

Pin number	Signal	Signal type	Pin number	Signal	Signal type
1	BUZZER	O_1	2	PWRGOOD_IN	I_2
3	Codec_AC97_CLK	O_1	4	V_BATT	P_2
5	Codec_SDATA_OUT	O_1	6	NC	-
7	Codec_SDATA_IN	I_1	8	GND	P
9	Codec_BIT_CLK	I_I	10	CRT-R	O_A
11	Codec_SYNC	O_1	12	CRT-G	O_A
13	Codec_RESET#	O_1	14	CRT-B	O_A
15	GND	P	16	GND	P
17	Lan TX-	O_2	18	CRT-HSYNC	O_1
19	Lan TX+	O_2	20	CRT-VSYNC	O_1
21	Lan RX-	O_2	22	3.3V	P
23	Lan RX+	O_2	24	TFT-R5	O_1
25	Lan LNLED#	O_3	26	TFT-R4	O_1
27	Lan LNKLED#	O_3	28	TFT-R3	O_1
29	3.3V	P	30	TFT-R2	O_1
31	USB[1]+	O_{USB}	32	TFT-R1	O_1
33	USB[1]-	O_{USB}	34	TFT-R0	O_1
35	Overcurrent#	I_3	36	GND	P
37	USB[2]+	O_{USB}	38	TFT-G5	O_1
39	USB[2]-	O_{USB}	40	TFT-G4	O_1
41	GND	P	42	TFT-G3	O_1
43	DCD1#	I_1	44	TFT-G2	O_1
45	DSR1#	I_1	46	TFT-G1	O_1
47	RXD1	I_4	48	TFT-G0	O_1
49	RTS1#	O_1	50	3.3V	P
51	TXD1	O_4	52	TFT-B5	O_1
53	CTS1#	I_1	54	TFT-B4	O_1
55	DTR1#	O_1	56	TFT-B3	O_1
57	RI1#	I_1	58	TFT-B2	O_1
59	3.3V	P	60	TFT-B1	O_1
61	RXD2	I_4	62	TFT-B0	O_1
63	NC	-	64	GND	P
65	TXD2	O_4	66	TFT-HSYNC	O_1
67	NC	-	68	TFT-VSYNC	O_1
69	3.3V	P	70	TFT-DE	O_1
71	Spare	-	72	TFT-SCLK	O_{PC}
73	GND	P	74	GND	P
75	NC	-	76	NC	-
77	NC	-	78	DIGON	O_1
79	NC	-	80	3.3V	P
81	NC	-	82	3.3V-Standby	P
83	GND	P	84	Power Button#	I_7
85	AD[00]	I/O	86	Internal use	-
87	AD[01]	I/O	88	NC	-
89	AD[02]	I/O	90	NC	-
91	AD[03]	I/O	92	NC	-
93	AD[04]	I/O	94	PS_ON#	O_5
95	AD[05]	I/O	96	NC	-
97	AD[06]	I/O	98	GND	P
99	AD[07]	I/O	100	LAD[3] *	I/O
101	AD[08]	I/O	102	LAD[2] *	I/O
103	C/BE[0]#	I/O	104	LAD[1] *	I/O
105	AD[09]	I/O	106	LAD[0] *	I/O
107	AD[10]	I/O	108	LDRQ# *	I_4

109	AD[11]	I/O	110	LFRAME#	O_1
111	AD[12]	I/O	112	LPCPD#	O_1
113	AD[13]	I/O	114	SERIRQ#	I/O_1
115	AD[14]	I/O	116	3.3V	P
117	C/BE[1]#	I/O	118	USB[3]+	O_{USB}
119	AD[15]	I/O	120	USB[3]-	O_{USB}
121	LOCK#	I/O_1	122	3.3V	P
123	PERR#	I/O_1	124	I²C_CLK	I/O_2
125	DEVSEL#	I/O_1	126	I²C_DAT	I/O_2
127	SERR#	I/O_1	128	GND	P
129	STOP#	I/O_1	130	IDE_DASP	I/O_3
131	NC	-	132	IDE_PDIAG	I/O_3
133	TRDY#	I/O_1	134	3.3V	P
135	IRDY#	I/O_1	136	IDE_CS3#	I/O_1
137	FRAME#	I/O	138	IDE_CS1#	I/O_1
139	AD[16]	I/O	140	IDE_A2	I/O_1
141	C/BE[2]#	I/O	142	IDE_A0	I/O_1
143	AD[17]	I/O	144	IDE_A1	I/O_1
145	PAR	I/O_1	146	GND	P
147	AD[18]	I/O	148	IDE_INTRQ	I_8
149	AD[19]	I/O	150	IDE_AK#	I/O_1
151	AD[20]	I/O	152	IDE_RDY	I/O_1
153	AD[21]	I/O	154	IDE_IOR#	I/O_1
155	AD[22]	I/O	156	IDE_IOW#	I/O_1
157	AD[23]	I/O	158	IDE_DRQ	I/O_1
159	C/BE[3]#	I/O	160	GND	P
161	AD[24]	I/O	162	IDE_D0	I/O_1
163	AD[25]	I/O	164	IDE_D1	I/O_1
165	AD[26]	I/O	166	IDE_D2	I/O_1
167	AD[27]	I/O	168	IDE_D3	I/O_1
169	AD[28]	I/O	170	IDE_D4	I/O_1
171	AD[29]	I/O	172	3.3V	P
173	AD[30]	I/O	174	IDE_D5	I/O_1
175	NC	-	176	IDE_D6	I/O_1
177	AD[31]	I/O	178	IDE_D7	I/O_1
179	REQ1# (used by onboard Ethernet)	I_6	180	IDE_D8	I/O_1
181	GNT1# (used by onboard Ethernet)	O_4	182	IDE_D9	I/O_1
183	REQ0#	I_6	184	IDE_D10	I/O_1
185	GNT0#	O_4	186	GND	P
187	RST#	O_1	188	IDE_D11	I/O_1
189	CLK0	O_1	190	IDE_D12	I/O_1
191	CLK1	O_1	192	IDE_D13	I/O_1
193	CLK2	O_1	194	IDE_D14	I/O_1
195	NC	-	196	IDE_D15	I/O_1
197	INTA#	I_6	198	HDRST#	O_6
199	INTB#	I_6	200	GND	P

Note * If the LPC interface is not used on the customers backplane, then the signals LAD[0..3] and LDRQ# have to be connected together and pulled-up to 3.3V with an 15kΩ resistor.

11.1 *Signal Type designators*

- I1 Input, TTL compatible.
- I_2 Input, low active with open collector/button.
- I_3 Input, TTL compatible with Schmitt-Trigger. Internally pulled up (15kΩ).
- I_4 Input, TTL compatible. Internally pulled up (15kΩ).
- I_5 Input, TTL compatible. Internally pulled down (15kΩ).
- I_6 Input, TTL compatible. Internally pulled up (6,8KΩ).
- I_7 Input, TTL compatible with Schmitt-Trigger and 16ms debounce. Internally pulled up (15kΩ).
- I_8 Inpul, TTL compatible. Internally pulled up (10kΩ).
- O_1 Output 3,3V (3,14V-3,46V), source 2mA, sink 5mA.
- O_2 Output, differential pair.
- O_3 Output, open collector. 5V tolerant.
- O_4 Output. Do not pull up or down externally!
- O_5 Output. Internally pulled up (15kΩ).
- O_6 Output. Internally pulled down (1kΩ).
- O_A Output, analog.
- O_{USB} Output. Internally pulled down (15kΩ).
- O_{PC} Clock Output. Target impedance 70Ω.
- I/O Input/Output.
- I/O_1 Input/Output. Internally pulled up (6,8kΩ).
- I/O_2 Input/Output. Internally pulled up (10kΩ).
- I/O_3 Input/Output (see X-board Design Guide).
- P Power Input.

12. APPENDIX E: JIDA STANDARD

12.1 *JIDA Information*

To obtain information about boards that follow the JIDA standard, use the following procedure.

1) Call Get BIOS ID with CL=1.
   The name of the first device installed will be returned.
   If you see the result **Board exists** (CL=0), increment CL, and call **Get BIOS ID** again.

2) Repeat until you see **Board not present** (CL≠0).
   You now know the names of all boards within your system that follows the JIDA standard.

3) You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes.
Do not rely on any association between board and board number.
Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai110.zip folder, which is available from the Kontron Embedded Modules Web site, for further information on implementing and using JIDA calls with C sample code.

13. APPENDIX F: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

13.1 *Buses*

13.1.1. Low Pin Count Bus (LPC)

- Low Pin Count Bus Specification, Aug. 2002, Intel

13.1.2. ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

13.1.3. PCI/104

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

13.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

13.3 Ports

13.3.1. RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

13.3.2. Serial ATA

- Serial AT Attachment (ATA) Working Group
  This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
  We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

13.3.3. USB

- USB Specification
  USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

13.4 *Programming*

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

14. APPENDIX G: DOCUMENT-REVISION HISTORY

Filename	Date	Edited by	Alteration to preceding revision
xbd1m010.doc	10.12.02	M. Unverdorben	Initial Preliminary Release
xbd1m011.doc	04.02.03	M. Unverdorben	Edit Interface Spec.
xbd1m012.doc	05.02.03	D. Gunter	Kontron Format and English Proofreading
Xbd1m013.doc	10.02.03	M. Unverdorben	Added Resource list, watchdog info, JIDI description
Xbd1m014.doc	22.02.03	M. Unverdorben	Added limitations, BIOS, Pin out table
Xbd1m110.doc	24.03.03	M. Unverdorben	Added power consumption
Xbd1m111.doc	01.07.03	M. Unverdorben	Added AMP 1.2 chapter, removed limitations: JRC setup screen and APM functions, exchanged summary screen picture, changed BIOS description to current BIOS version, corrected Pinout list
Xbd1m112.doc	25.07.03	C. Hoch	Added signal type in Pinout list and Note for LPC.
Xbd1m113.doc	15.10.03	D. Gunter	Added USB CD-ROM boot support statement. Changed serial port description. Added initial delay information to watchdog section. Changed PCI INTC# and PCI INTD# description in PCI configuration of BIOS menu. Added “Legacy USB configuration” section to “Miscellaneous Configuration” menu in the BIOS description section. Added “Memory Optimization” and “LPC Bus” menu in the BIOS description section.
Xbd1m114.doc	20.01.04	D. Gunter	Added information about TV Output support and removed UDMA/DMA information. Changed default setting of “Flat Panel Mode” in BIOS setup from disabled to enabled.
Xbd1m115.doc	15.03.04	D. Gunter	Added Strap Pins section 6.16.2
Xbd1m116.doc	16.03.04	D. Gunter	Changed Pin assignments for Pins 43, 45, 49, 53, 57, 63, and 67 in X-board connector pinout table to reflect COM port configuration. Check pinout table for changes.
Xbd1m117.doc	25.03.04	D. Gunter	Updated and changed information in section 3.3.4 Added information to section 3.4.1.
Xbd1m118.doc	26.05.04	D. Gunter	Removed Video Overlay information from VGA output section 6.9.
Xbd1m119.doc	08.07.04	D. Gunter	Changed Serial description in section 6.5 and removed information from section 6.15.1.
Xbd1m120.doc	05.08.04	D. Gunter	Added additional Strap Pins to section 6.16.2