SR003AN/D

Compensation for Linear Regulators

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APPLICATION NOTE

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In the majority of low drop and quasi low drop (composite NPN–PNP) regulators, the pass device or the pass device driver, is a lateral PNP transistor. The lateral PNP transistor is inherently a low frequency cutoff device with a poor transient response. An external capacitor must be connected between the output and ground to provide filtering and compensation.

This application note discusses the role of the output capacitor in loop stability. Guidelines for selecting an appropriate capacitor are provided.

Introduction

There is little specific information available on choosing the correct type and value of compensation capacitor for low and quasi low drop out linear regulators. Many designers simply use the one shown in the application diagram of the device data sheet without worrying about how and why that value was selected.

The Role of the Output Capacitor

The compensation capacitor value cited in most linear regulator data sheets has a large safety factor built in. It is not necessarily the cheapest or the best solution for a particular application.The compensation capacitor determines three key characteristics of a linear regulator's performance: start–up delay, load transient response and loop stability. Start–up delay and transient response can be considered together since they are so closely related.

A large capacitor takes a long time to charge up. The charging period $T_{Startup}$, is:

$$T_{Startup} = \frac{CV_{OUT}}{I_{LIMIT}}$$

where V_{OUT} is the regulator's output voltage, I_{LIMIT} is the current limit of the regulator and C is the value of the capacitor. If the capacitor is completely discharged before the regulator is powered up, the regulator will current limit during start–up and the rise in the output voltage will be delayed. The larger the value of the capacitor, the longer it will take the output voltage to reach its nominal value.

Conversely, if the capacitor is too small, the output voltage will overshoot its nominal value during startup. The regulator's internal control loop can't respond quickly enough to limit the output voltage. If the overshoot is large enough, it may damage sensitive electronics tied to the regulator's output.

Since it is impossible to investigate all three key characteristics at once, the designer should concentrate on achieving a stable loop design first and then check the start up delay and the load transient response.

Loop Stability

A simplified block diagram of a low drop linear regulator is shown in Figure 1. It consists of three basic parts:

1. A voltage reference, V_{REF}, which is independent of temperature and supply voltage.
2. An error amplifier that compares the voltage reference to a sample of the output voltage and generates a signal proportional to their difference.
3. A series pass device that provides the output current to the load and regulates the output voltage.

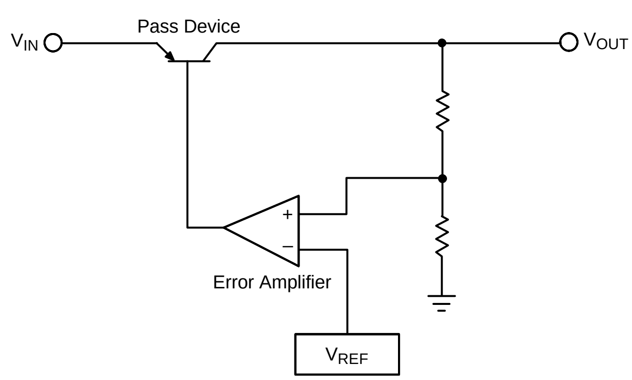

Figure 1. Simplified Low Dropout Linear Regulator Block Diagram

A well designed feedback system has a closed loop response that ensures unconditional stability. An ideal system (Figure 2) has a single pole response that determines the system's crossover frequency. Its crossover frequency (f_C) is chosen to ensure that the system can quickly respond to load transients without undue ringing (oscillation). To ensure this stability, the phase margin must be at least 30° away from 360° at f_C (Figure 2).

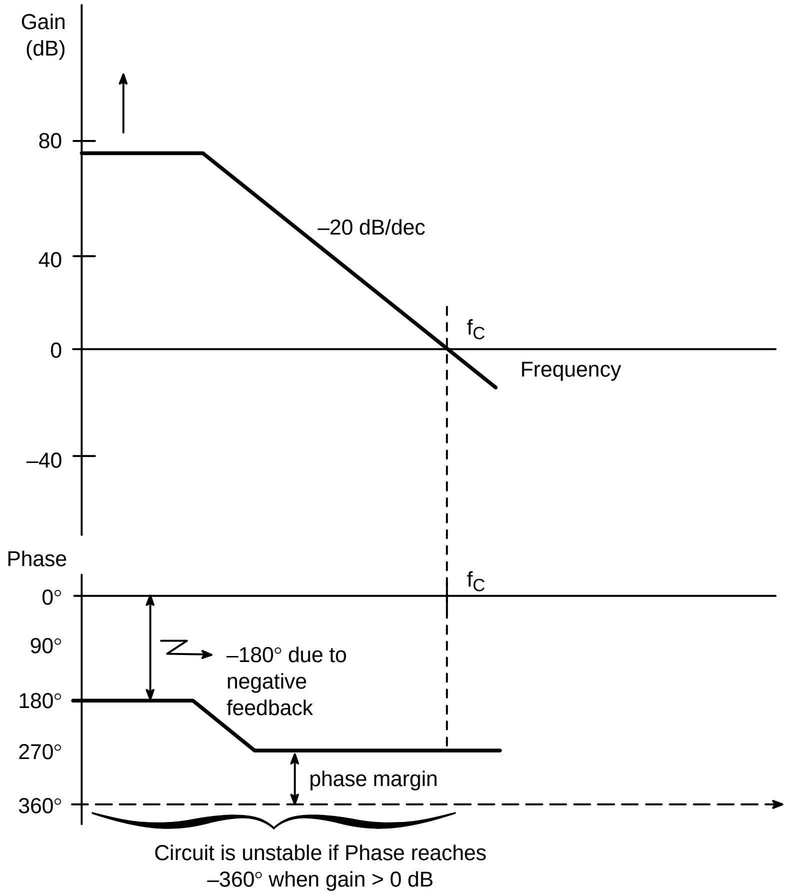

Figure 2. Bode Plot of an Ideal System with a Single Pole Response

Unlike the ideal system described above, a low drop linear regulator usually has three dominant poles. Two poles are set by the regulator's design. The third is a function of the regulator's load and output capacitor. The ESR (equivalent series resistance) of the output capacitor adds a zero to the loop.

The first pole is determined by the error amplifier. It occurs between 10 Hz and 300 Hz. The second pole is due to the frequency response of the PNP pass device or the PNP bias device in a compound regulator. It usually occurs between 100 kHz and 300 kHz, depending on load conditions. The third pole, set by the output capacitor and the load, occurs within the same frequency range as the error amplifier pole. It shifts as the load changes. If the load is light enough, it may even be located below the error amplifier pole.

A simplified load for a regulator is shown in Figure 3. Its transfer function is:

$$Z_L(s) = \frac{\left(ESR + \frac{1}{sC}\right)R_L}{R_L + ESR + \frac{1}{sC}} = \frac{R_L(1 + ESR \times sC)}{1 + sC(R_L)} = \frac{1 + Z_1}{1 + P_1} \quad (1)$$

The load pole frequency is

$$f_P = \frac{1}{2\pi(R_L + ESR)C} \quad (2)$$

The capacitor zero frequency is

$$f_P = \frac{1}{2\pi(ESR)C} \quad (3)$$

In comparing the denominator's of equations 2 and 3, it is apparent that a capacitor with a large ESR value may cause a zero close to either the load or the error amplifier pole and cancel it out. This may destabilize the circuit and cause oscillations on the output.

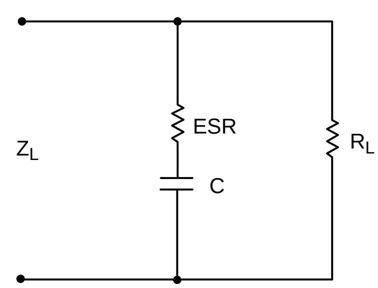

Figure 3. The Linear Regulator's Load Includes a Compensation Capacitor and Load Resistor R_L. ESR Represents the Equivalent Series Resistance of the Capacitor

Figure 4 shows the SPICE plots of the main output V_{OUT1} of the CS8156 dual regulator from ON Semiconductor. In Figure 4, the capacitor has an ESR of 3.0 Ω and results in a marginally stable design. In Figure 5, the ESR is reduced to 1.0 Ω and its design is stable for the 120 Ω load.

A perfect capacitor (almost zero ESR) may cause a problem with loop stability since the zero due to the ESR is at a high frequency. The gain slope falls at a rate of –40 dB per decade (–2.0 slope) to 0 dB before the capacitor zero can effect the slope. The Spice plot in Figure 6 illustrates the problem with using a "perfect" 22 μF capacitor on the output of the CS8156. The gain falls to zero at approximately 8.0 kHz with almost no phase margin.

Tantalum and aluminum electrolytic capacitors have higher ESRs and therefore are better for compensating than film capacitors with their lower ESRs.

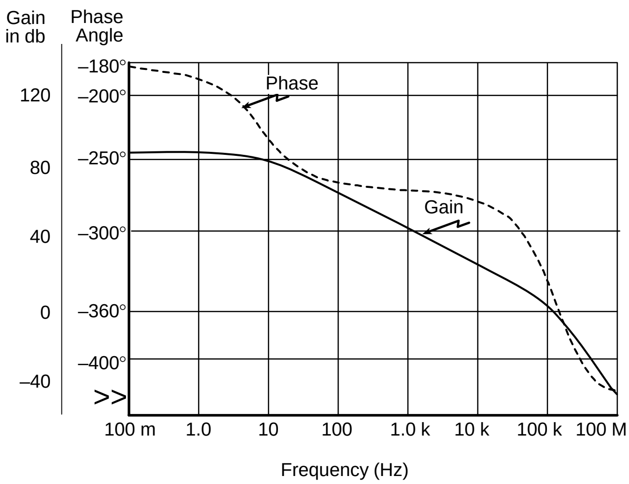

Figure 4. Bode Plot of the Output of the CS8156 SMART REGULATOR®. The Load Consists of the R_{OUT} = 120 Ω and C_{OUT} 22 μF with ESR = 3.0 Ω. The Output is Marginally Stable.

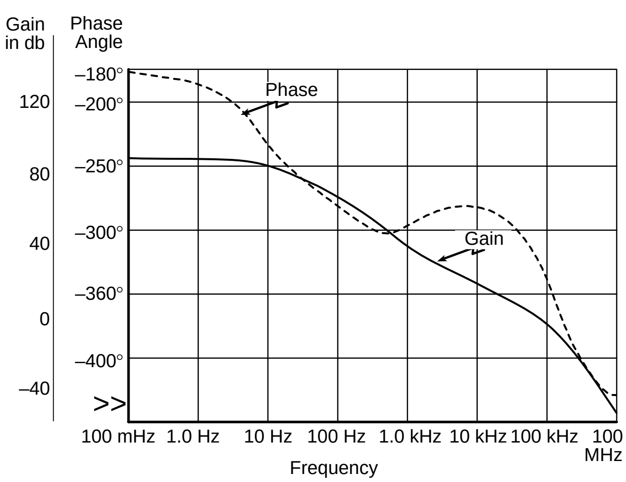

Figure 5. Bode Plot of CS8156, R_{OUT} = 120 Ω, C_{OUT} 22 μF, ESR = 1.0 Ω. Note thet the ESR of the Capacitor has been Reduced to 1.0 Ω. The Output is Stable.

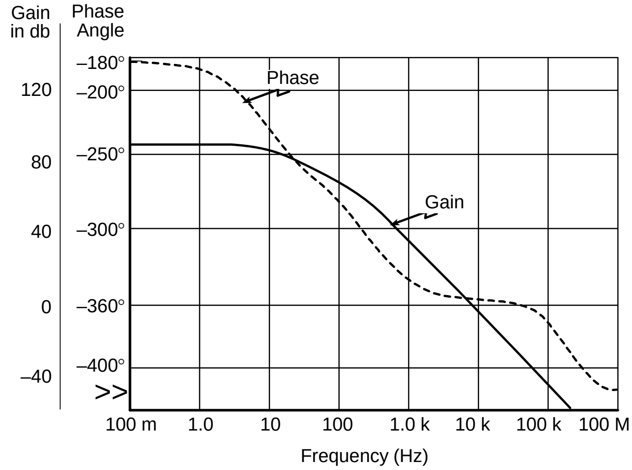

Figure 6. Bode Plot of CS8156, R_{OUT} = 120 Ω, C_{OUT} 22 μF, ESR = 0.01 Ω. Reducing the ESR to 0.0 Ω. Results in Almost Zero Phase Margin. The System is Unstable.

Electrolytic Capacitors

An equivalent circuit for an electrolytic capacitor is shown in Figure 7 where

C = Capacitance
R_S = Series Resistance
L = Inductance
R_P = Parallel Resistance

This equivalent circuit can be further simplified so that all losses, both series and parallel, are added together at one point and treated as one resistor, the equivalent series resistance or ESR. The equivalent circuit is thus reduced to an RC circuit as shown in Figure 8. The ESR changes the impedance of the capacitor since it has the same effect as adding an external resistor in series.

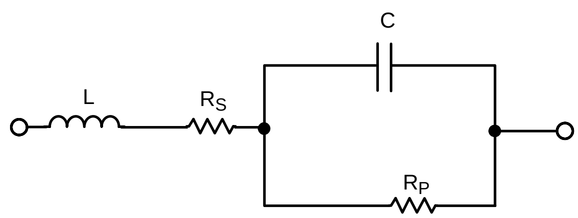

Figure 7. Equivalent Circuit for Electrolytic Capacitor

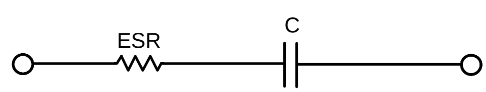

Figure 8. Simplified Equivalent Circuit for Electrolytic Capacitor

Most aluminum capacitors are unsuitable for applications where they will be exposed to temperature extremes. Although the ESR varies slightly between 25°C and 85°C, at low temperatures it can increase by a factor of up to 30 times and at high temperatures, its electrolyte may evaporate.

Figures 9 through 11 show typical aluminum electrolytic capacitor characteristics over frequency and temperature. The variations are usually less in capacitors with higher voltage ratings.

If the regulator is expected to operate over an extreme temperature range (–40°C to +125°C) , a tantalum or film capacitor may be the only appropriate choice.

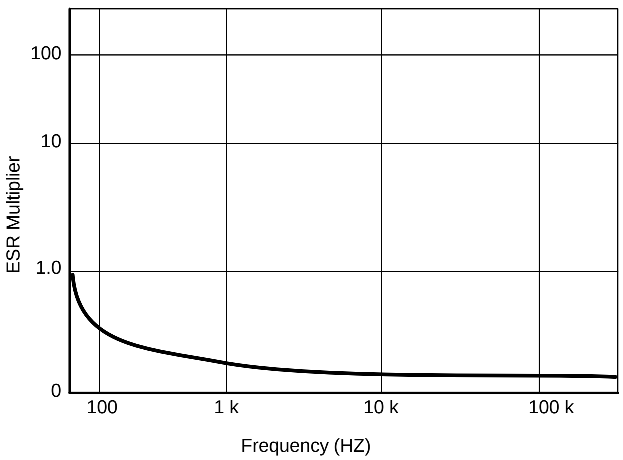

Figure 9. ESR vs. Frequency for Typical Aluminum Electrolytic Capacitor

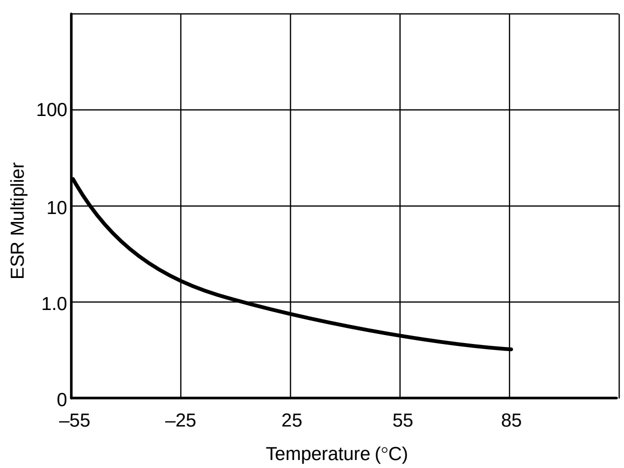

Figure 10. ESR vs. Temperature for Typical Aluminum Electrolytic Capacitor

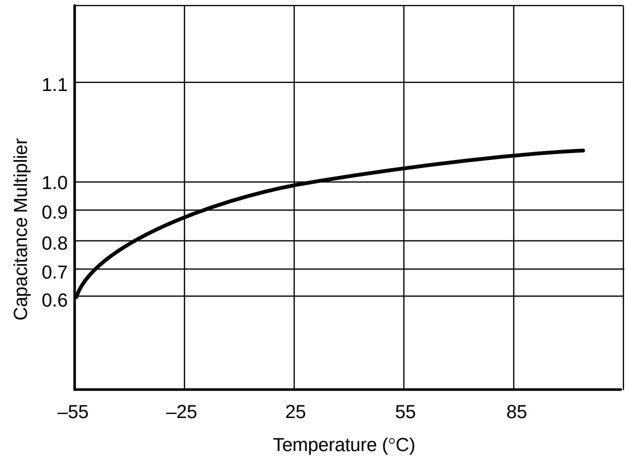

Figure 11. Capacitance vs. Temperature for a Typical Aluminum Electrolytic Capacitor

Stability Considerations

The stability of the regulator depends on the following factors:

1. **Load** – Most regulators are more unstable when operated in their low to medium load range, e.g., 100 mA for a 500 mA regulator.
2. **Output Capacitor Value** – In general the higher the value of output capacitor, the more stable the regulator will be.
3. **Capacitor ESR** – In general a capacitor with low ESR will improve the stability of the design.
4. **Temperature Range** – At lower temperatures the loop gain increases, capacitor ESR increases and capacitance value decreases. These value changes shift the poles of the feedback loop, increasing gain and decreasing phase margin. The system tends toward instability.
5. **Supply Voltage** – At higher input voltages, the loop gain increases adding to the instability.

Selecting the Right Capacitor Value

The output current range, temperature, and supply voltage ranges are all known for a particular design. A capacitor value and type is chosen based on cost, availability, size, and temperature constraints. A good starting point is the IC manufactures’ recommended value. To determine an acceptable ESR, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

A system designer can not easily tell exactly where the dominant poles are for a given regulator, but using the following procedure a designer can build a stable power supply for an application.

Step 1: Place the completed circuit with a tantalum capacitor of the manufacturers recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor.

(Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear (Figures 12 and 13). Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

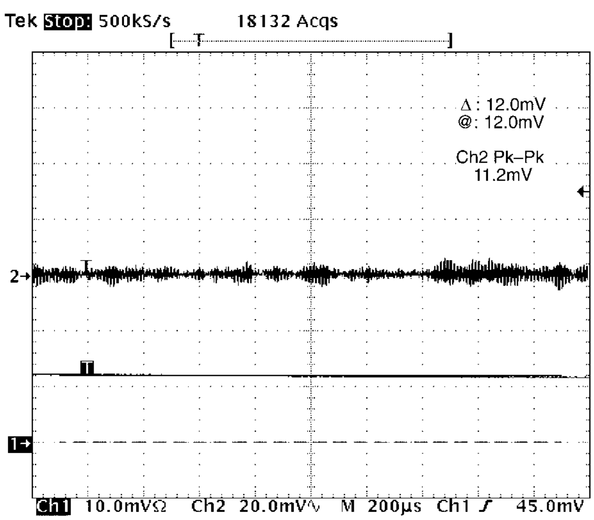

Figure 12. Oscilloscope Tracing of I_{OUT} (1) and V_{OUT} (2). The Capacitor is a 22 μF with 15 Ω ESR. Note the Small of Oscillations (11 mV_{P-P}) About V_{OUT}

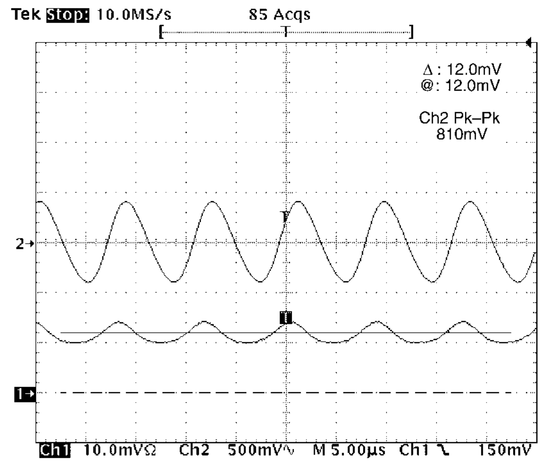

Figure 13. Oscilloscope Tracing of I_{OUT} (1) and V_{OUT} (2). The Capacitor is a 22 μF with 20 Ω ESR. Note the Dramatic Increase in the Amplitude of the Oscillations (810 mV_{P-P}) about V_{OUT} when the ESR is Changed from 15 Ω (Figure 12) to 20 Ω

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing. Figure 14 shows the transient response of the CS8156 with a 22 μF capacitor and an ESR of 3.0 Ω and 1.0 Ω on V_{OUT1}. I_{LOAD} is switching between 0.12 A and 0.35 A.

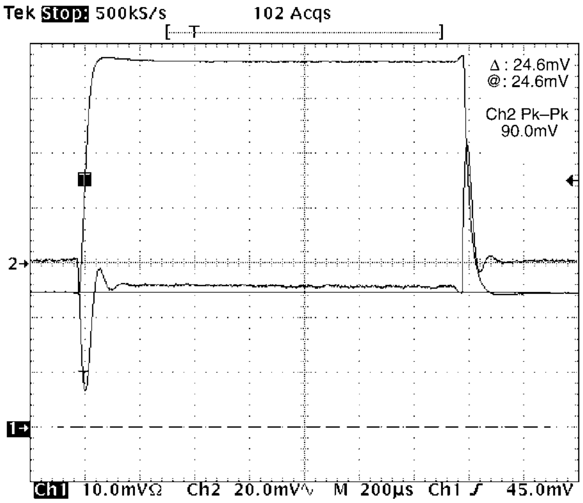

Figure 14. Oscilloscope Tracing for I_{LOAD} (Ch1) and V_{OUT} (Ch2). The Capacitor is a 22 μF with 3.0 Ω ESR. When I_{LOAD} is Switched From 120 mA to 350 mA, the Output Voltage Dips, Overshoots and then Recovers.

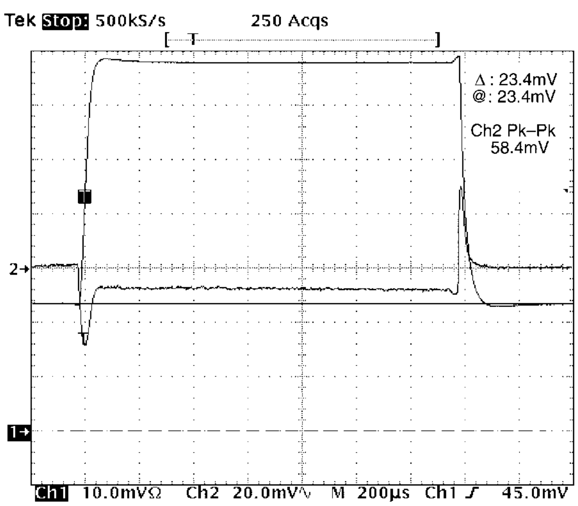

Figure 15. Oscilloscope Tracing for I_{LOAD} (Ch1) and V_{OUT} (Ch2). The Capacitor is a 22 μF with 1.0 Ω ESR. With the Lower ESR, V_{OUT} Shows No Measurable Overshoot During Recovery From the Switching Transient at the Load

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Do the oscillations increase with temperature? They shouldn’t. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Conclusion

Many designers use the compensation capacitor value specified in the regulator data sheet. While this value may be adequate for many applications, it may not be optimal. Problems arising from inappropriately chosen capacitors are most apt to appear during regulator power up and under low temperature, light load conditions.

Avoiding these problems simply requires a few easy tests to ascertain correct capacitor values and ESRs under the applications expected operating conditions.

Notes

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