

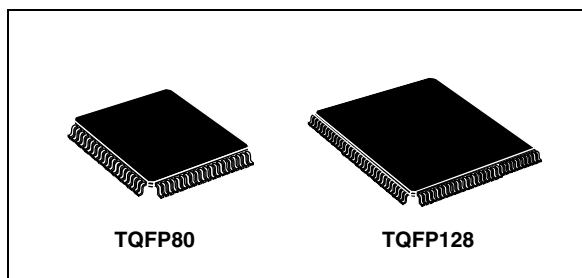


STR91xxA, STR91xxB

ARM966E-S™ 16/32-Bit Flash MCU with Ethernet, USB, CAN, AC Motor Control, 4 Timers, ADC, RTC, DMA

PRELIMINARY DATA

- **16/32-bit 96 MHz ARM9E based MCU**
 - ARM966E-S RISC core: Harvard architecture, 5-stage pipeline, Tightly-Coupled Memories (SRAM and Flash)
 - STR91xx implementation of core adds high-speed burst Flash memory interface, instruction prefetch queue, branch cache
 - Up to 80 MIPS directly from Flash memory
 - Single-cycle DSP instructions are supported
 - Binary compatible with 16/32-bit ARM7 code
- **Dual Burst Flash Memories, 32-bits wide**
 - 256KB/512KB Main Flash, 32KB 2nd Flash
 - Sequential Burst operation up to 75 MHz
 - 100K min erase cycles, 20 yr min retention
- **SRAM, 32-bits wide**
 - 64K or 96K bytes, optional battery backup
- **9 Programmable DMA channels**
 - One for Ethernet, eight programmable chnls
- **Clock, Reset, and Supply Management**
 - 4-25MHz external, internal PLL to 96 MHz
 - Real-time clock provides calendar functions, tamper detection, and wake-up functions
 - Reset Supervisor monitors voltage supplies, watchdog timer, wake-up unit, ext. reset
 - Brown-out monitor for early warning interrupt
 - Run, Idle, and Sleep Mode as low as 50 uA
- **Vectored Interrupt Controller (VIC)**
 - 32 IRQ vectors, 30 intr pins, any can be FIQ
 - Branch cache minimizes interrupt latency
- **8-channel, 10-bit A/D Converter (ADC)**
 - 0 to 3.6V range, 2 usec conversion time



- **11 Communication Interfaces**
 - 10/100 Ethernet MAC with DMA and MII port
 - USB 2.0 Full Speed (12 Mbps) slave device
 - CAN interface (2.0B Active)
 - 3 16550-style UARTs with IrDA protocol
 - 2 Fast I²C™, 400 kHz
 - 2 channels for SPI™, SSI™, or Microwire™
 - 8/16-bit EMI bus on 128 pin packages
- **Up to 80 I/O pins (muxed with interfaces)**
 - 5V tolerant, 16 have high sink current (8mA)
 - Bit-wise manipulation of pins within a port
- **16-bit Standard Timers (TMR)**
 - 4 timers each with 2 input capture, 2 output compare, PWM and pulse count modes
- **3-Phase Induction Motor Controller (IMC)**
 - 3 pairs of PWM outputs, adjustable centers
 - Emergency stop, dead-time gen, tach input
- **JTAG Interface with Boundary Scan**
 - ARM EmbeddedICE® RT for debugging
 - In-System Programming (ISP) of Flash
- **Embedded Trace Module (ARM ETM9)**
 - Hi-speed instruction tracing, 9-pin interface

Device Summary

Features	STR9164A-96U6	STR9175A-96U6	STR9164B-96H6	STR9175B-96H6	
FLASH memory - Kbytes	256+32	512+32	256+32	512+32	
RAM - Kbytes	64	96	64	96	
Peripheral Functions	USB, CAN, 48 I/Os		Ethernet, USB, CAN, EMI, 80 I/Os		
Operating Voltage	Two supplies required. Core: 1.8V +/-10%, I/O: 2.7V to 3.6V				
Operating Temperature	-40 to +85°C				
Packages	TQFP80, 12x12mm		TQFP128, 14x14mm		

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1/69

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.